ADM1270 Hotswap controller Design Guide

By Glenn Morita
[glenn.morita@analog.com]

Note: The section titles correspond to the design tool sections.

System Specifications

The following conditions are assumed for this example:

- Controller = ADM1270
- V_{IN} = 32 V Nominal
- V_{IN} = 20 V Minimum
- 18V Power Good Threshold
- 8.7V UV Threshold
- 37.5V OV Threshold
- V_{MAX} = 55V
- I_{TRIP} = 450 mA
- C_{LOAD} = 100 µF
- T_{AMAX} = 60°C
- $R_{POWERUP}$ = 500Ω (static load resistance during system power up)

To simplify this example, the calculations exclude the effects of component tolerances. These tolerances should of course be considered when designing for worst-case conditions. Note also there may be slight differences in the numbers quoted here compared to the design tool. In this case the tool takes precedence.

Sense Resistor/Vdrop Selection Tool Section 2

The sense resistor chosen is primarily based on the required circuit breaker trip current. However, the ADM1270 has an adjustable current limit threshold which allows for fine tuning of the current limit beyond that provided by the limited availability of standard sense resistor values. The sense voltage can be programmed within a 12.5 to 62.5 mV range. Such a low sense voltage, along with the flexibility of programmability, offers reduced power loss and size in sense resistor selection.

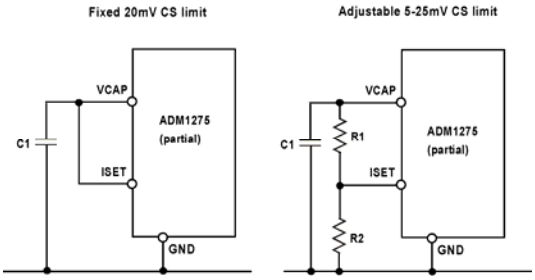
The circuit breaker timer (current fault glitch filter) begins is typically 1mV below the regulation point. This means that to set a trip point of 450 mA(45mV) we need to set the regulation point to ~460 mA (46mV).

$$R_{SENSE} = \frac{V_{SENSE}}{I_{TRIP}} = \frac{0.050\,\text{V}}{450\,\text{mA}} \approx 110m\Omega$$

This is not a common available value so the closest to consider is 100mΩ. Lets reverse the equation above to determine the required sense voltage.

$$V_{SENSE} = R_{SENSE} \times I_{TRIP}$$
$$= 100m\Omega \times 0.45 \approx 45mV$$

The ISET pin can be programmed to a desired voltage using a divider from the VCAP reference. ISET voltage = Vsense x 40.



$$V_{ISET} = V_{SENSE} \times 40 = 45mV \times 40 = 1.80V$$

Using the VCAP reference of 3.6V and assuming R2= 100KΩ, this will result in a top resistor of 100 KΩ.

The given ISET voltage provides a circuit breaker trip point of ~450 mA and a regulation current set point of 460 mA.

Power Rating:

Assuming worst case DC current could be as high as 487 mA (including tolerances), Therefore power can be calculated as:

$$P_{RSENSE} = I_{TRIP}^{\ 2} \times R_{SENSE}$$
$$= (0.487\ \text{A})^2 \times 0.10\ \Omega$$
$$=\sim 0.024\ \text{W}$$

So the sense resistor should be capable of dissipating 0.024 W (including temperature derating factors). A 0.1W or 0.125W resistor is recommended.

Summary of the key component selection for this section:

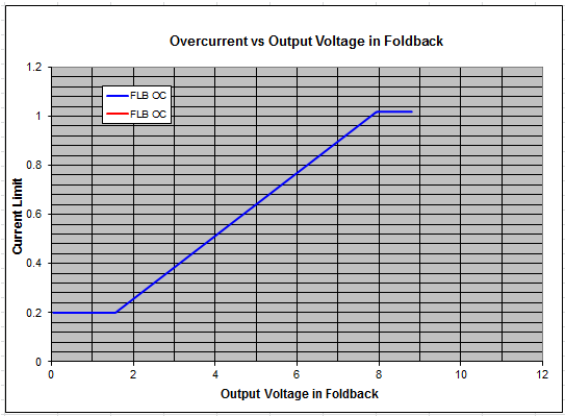
$R_{ISET(TOP)}$ = 100 KΩ

$R_{ISET(BOT)}$ = 100 KΩ

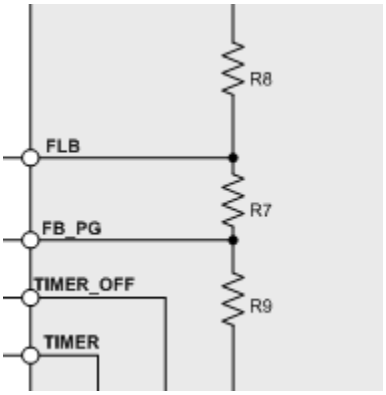
R_{SENSEx} = 100mΩ

PG and Foldback - Tool Section 3

The ADM1270 utilizes a foldback technique to protect the MOSFETs in the event of overcurrent faults or short circuits. The output voltage is monitored using a divider on the FLB pin and the current limit is adjusted based on the V_{DS} of the MOSFET. An example of this relationship can be seen in figure x



When the output voltage is at zero, there is a lower limit clamp to prevent the current limit approaching zero. This clamp is fixed at 0.2V on the FLB pin (or 8mV Vsense), which equated to ~200mA on this particular design. As the output voltage increases, the current limit ramps as a function of the output voltage. This threshold is set by the divider on the FLB pin, using a reference equal to $V_{SENSEREG}$ X 40. This voltage should be chosen to be low enough to avoid any expected Vout load steps from affecting the current limit. Also, the PGOOD output is derived from the voltage divider that sets the FLB level.



Targeting 8V and an 11V PGOOD we get a divider of 95.3KΩ (R8), 4.02K (R7), and 10KΩ (R9).

Summary of the key spec / component selection for this section:

V_{PG}	= 18V
V_{FLB}	= 13.2V
R7	= 4.53K
R8	= 332K
R9	= 20K

MOSFET Selection - Tool Section 6

The first consideration as criteria for selection of a suitable MOSFET is the R_{DSON} specification, to ensure that minimum power is lost in the MOSFET when it is fully enhanced in normal operation.

The ADM1270 features a high voltage gate drive to ensure a minimum of 10V V_{GS} is achieved to maintain the lowest specified R_{DSON}. The gate drive circuit is designed to achieve this while still ensuring the 20V maximum V_{GS} spec is not violated.

As the temperature of the MOSFET increases, its power rating is reduced, or *derated*. The R_{DSON} spec determines the maximum junction temperature of the MOSFET and therefore the required derating can be applied to SOA parameters. In addition, running MOSFETs at high temperatures may decreases their reliability.

Lets begin by estimating the required R_{DSON}. Recall the maximum DC current was 487mA,

worst case. Then using the maximum ambient temperature specified in section 1 we can estimate the power loss in the MOSFET(s). First we make a few assumptions…

- R_{thJA} = 78 C/W (must not exceed)
- T_{jMAX} = 120 °C

  (This is the maximum preferred junction temp, keeping well away from any silicon limits)

Calculate the junction temperature rise:

$$T_{RISE} = T_{jMAX} - T_{AMAX} = 120 - 60 = 60^{\circ}\text{C}$$

Then the power for a single FET:

$$P_{MOSFET} = \frac{T_{RISE}}{R_{thJA}} = \frac{60}{78} = 770mW$$

Now total R_{DSON}:

$$R_{DSON} = \frac{P_{MOSFET}}{I_{MAXDC}^{\ 2}} = \frac{0.770}{0.487^2} = 3.25\Omega$$

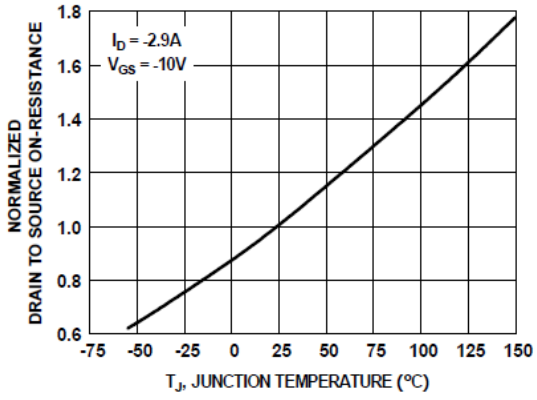
Now we derate this further by a factor of 1.6:

$$R_{DSON} = \frac{3.25}{1.6} = 2.03\Omega$$

Taking this as our target R_{SDON} we can now search for suitable candidates. The search can be narrowed to FETs that fit the following profile:

- V_{DS} = 60V (55V may be possible but not preferred)
- V_{GS} = 20V
- $R_{DSON} \leq 2.03\Omega$

After selecting a suitable MOSFET, the derating of the R_{DSON} should be quantified using the MOSFET datasheet graph of R_{DSON} against T_J.



Using T_{jMAX} of 120 °C, we can see the R_{DSON} increases by a factor of 1.6 to about 220mΩ (assuming 135mΩ at 25°C) at 120°C. As a rule it is best to keep junction temp ≤120C.

Assuming that the MOSFET's max R_{DSON} is 220mΩ, the power of the FET can be determined by:

$$\begin{aligned} P_{MOSFET} &= \left(I_{DMAX} \times 10\%\right)^2 \times R_{DSON} \\ &= \left(0.487\ \text{A}\right)^2 \times 220m\,\Omega \\ &\approx 52m\text{W} \end{aligned}$$

The MOSFET's thermal resistance at ambient temperature should be specified in the datasheet. The footprint size, airflow, nearby heat sources and additional copper will also have an effect on this value so care must be taken to ensure the specified conditions are met. Assume, for this design a target of:

$$R_{thJA} = 78^{\circ}\text{C/W}$$

(Note: Care should be taken to ensure layout/airflow does not exceed this figure)

As the MOSFET is expected to dissipate ~52mW, a worst-case temperature rise of 4.1 °C above ambient can be expected as follows:

$$T_{RISE} = R_{thJA} \times P_{MOSFET} = 4.1^{\circ}\text{C}$$

The resulting junction temp of the FET can be determined as follows:

$$T_J = T_A + T_{RISE} = 60 + 4.1 = 64.1^{\circ}\text{C}$$

As this is below the maximum selected value of 120°C, the risk of thermal runway should be avoided. When using multiple MOSFETs in parallel, a 10Ω resistor should be use in series with the gate of each MOSFET to prevent oscillations.

Summary of the key spec / component selection for this section:

Q_X	= Selected 135mΩ MOSFET.
R_{thJA}	= 78 K/W

Power Derating Factor

Now that the maximum junction temperature is verified we can determine the maximum derate factor. This number will be used to derate all the SOA parameters to verify a robust solution across temperature.

To determine the maximum expected case temperature we can use:

$$T_C = T_j - (R_{thJC} \times P_{MOSFET})$$

$$T_C = 64.1 - (78 \times 0.052) = 60^\circ C$$

Now the derating factor can be calculated as follows:

$$DF = \frac{T_{J\max} - T_{CSOA}}{T_{J\max} - T_{C\max}} = \frac{150°C - 25°C}{150°C - 60°C} = 1.4$$

Summary of the key spec / component selection for this section:

DF = 1.4

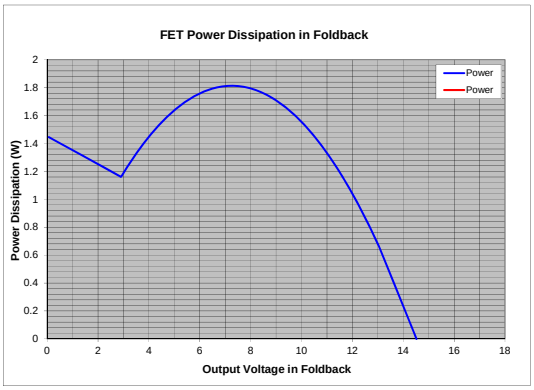
MOSFET SOA Analysis – Short Circuit

The next step is to review the SOA curve on the MOSFET datasheet to determine how much time it can tolerate the worst case power in the FET. This will determine a suitable timer capacitor value.

The ADM1270 has a very fast overcurrent detect circuit which detects a severe overcurrent event and responds in <300ns. There is also a very large gate pulldown device to ensure large MOSFET are shutdown fast. These combined should ensure ~1µs shutdown(excluding any system level component which may slow down di/dt) . The controller will re-establish control and begin controlled current fault timing.

If a short was applied the Vds of the FET can be assumed to be ~20V (assuming source at GND). In reality the number would likely to be lower than this due to line impedance.

However, if we look at the profile of the FET power against Vout we see that the relationship is not monotonic.



In figure x we can see that the worst case power in the FET is at ~7V (35% of Vin). The current can be easily calculated using the following equation:

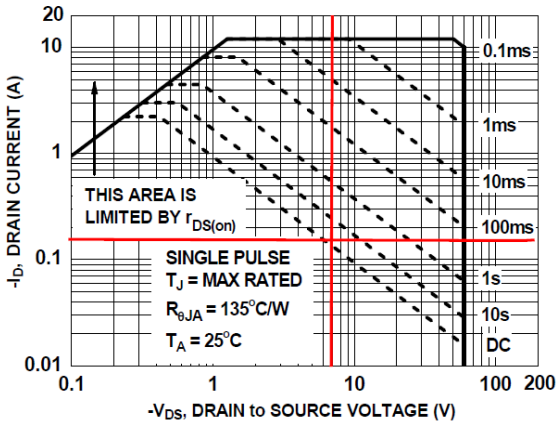
$$V_{FLB} = V_{OUT\_WCP}\left(\frac{R_{FLB\_BOT}}{R_{FLB\_TOP} + R_{FLB\_BOT}}\right)$$

$$= 7 \times \left(\frac{20}{20 + 336.5}\right) = 0.413$$

$$I_{FLB\_WCP} = \frac{V_{FLB}}{R_{SENSE} \times CS_{GAIN}} = \frac{0.413}{100m\Omega \times 40} = 103mA$$

(WCP=Worst Case Power)

Now derate this by 1.4 *(from section 5)* and we get 145mA. So if we go to the SOA diagram of the MOSFET, and intersect 7V with 145mA, we get approximately 10s. This means that timer "fault time" should never exceed 10s.



It should be noted that some FETs SOA power lines do not always represent a constant power product. This should be checked and if the line is not constant power then more points should be checked.

Summary of the key spec / component selection for this section:

T_{SOA_MAX} = 10s

Powerup analysis - Tool Section 5

Now that the timer had been selected, we must check to verify that there is sufficient time available to allow the loads caps to complete powerup. This is determined by how long the startup current profile intersects with the current limit… i.e. how long the timer is active during powerup.

During the *power-up* phase, the controller will usually hit the current limit due to the inrush current demanded by the load capacitance. If the time set by the TIMER pin is insufficient to allow the load capacitors to charge, then the MOSFET will be disabled and system will not power up.

We can use the following equation to estimate the powerup time using an average current limit across the foldback system:

$$t_{CHARGE} = \frac{C_{LOAD} \times V_{MAX}}{I_{AVERAGE} - \frac{V_{MAX}}{R_{POWERUP}}}$$

$$= \frac{100 \times 10^{-6}\ \text{F} \times 32\ \text{V}}{103\text{mA} - \frac{32}{1000}}$$

$$\approx 45ms$$

$T_{POWERUP}$ = ~ 45ms

Timer Capacitor - Tool Section 4

Now that the MOSFETs SOA requirements have been determined, and powerup time is satisfied, a TIMER capacitor value can be calculated. This can be calculated as follows:

$$C_{TIMER} = \frac{t_{TIMER} \times I_{TIMER}}{V_{TIMER}}$$

Where I_{TIMER} = 20 µA and V_{TIMER} = 2.0 V,

$$C_{TIMER} = \frac{\left(45 \times 10^{-3}\ \text{s}\right) \times \left(20 \times 10^{-6}\ \text{A}\right)}{2.0\ \text{V}}$$

$$\approx 0.45\ \text{uF}$$

Power in MOSFET at startup -SOA

Now, as a final step we need to check that the power being dissipated in the FETs at startup is within the SOA limits of the MOSFET. We can calculate the Energy required to charge the laod cap as follows:

$$E_{CL} = \frac{CV^2}{2}$$

$$= \frac{100 \times 10^{-6} \times (32)^2}{2}$$

$$\approx 0.052\ joules$$

The power can be determined using:

$$P_{FET} = \frac{E}{t}$$

$$= \frac{0.052}{45 \times 10^{-3}} \quad \text{(where t = 116ms)}$$

$$\approx 1.16W$$

Now calculate the current at max Vds…

$$I = \frac{P}{V} = \frac{1.16}{32} = 36mA$$

Now if we examine the SOA again, we can see that 32V and 36mA corresponds to ~10s. As the maximum expected powerup is ~45ms, there is adequate room for tolerance and margin within this spec.