CrossCore® Embedded Studio 1.0.1 Release Notes

Introduction

This document contains the release notes for CrossCore® Embedded Studio (CCES) version 1.0.1. It describes the release in detail and provides latest information that supplements the main documentation.

This release includes support for the processors listed in the next section, below.

Users of previous releases should check the "Version Compatibility" section, below, for pertinent instructions on modifying existing applications for this new release.

For product support assistance, please contact our Processor Tools Support Team at <processor.tools.support@analog.com>.

Update Highlights

Supported Processors

This release of CrossCore Embedded Studio adds support for the following processors:

- Blackfin Processors:
  - ADSP-BF504, ADSP-BF504F, ADSP-BF506F
  - ADSP-BF512, ADSP-BF514, ADSP-BF516, ADSP-BF518
  - ADSP-BF522, ADSP-BF524, ADSP-BF526, ADSP-BF523, ADSP-BF525, ADSP-BF527
  - ADSP-BF531, ADSP-BF532, ADSP-BF533,
  - ADSP-BF534, ADSP-BF536, ADSP-BF537
  - ADSP-BF538, ADSP-BF539
  - ADSP-BF542, ADSP-BF542M, ADSP-BF544, ADSP-BF544M, ADSP-BF547, ADSP-BF547M, ADSP-BF548, ADSP-BF548M, ADSP-BF549, ADSP-BF549M,
  - ADSP-BF561
  - ADSP-BF592-A
- SHARC Processors
  - ADSP-21160, ADSP-21161
  - ADSP-21261, ADSP-21262, ADSP-21266
  - ADSP-21362, ADSP-21363, ADSP-21364, ADSP-21365, ADSP-21366
  - ADSP-21367, ADSP-21368, ADSP-21369
  - ADSP-21371, ADSP-21375
  - ADSP-21467, ADSP-21469
  - ADSP-21477, ADSP-21478, ADSP-21479

    - ADSP-21483, ADSP-21486, ADSP-21487, ADSP-21488, ADSP-21489

As with CrossCore Embedded Studio 1.0.0, this release also supports the following Blackfin processors:

- ADSP-BF606, ADSP-BF607, ADSP-BF608, ADSP-BF609

Tools Enhancements

Dynamically Loadable Modules

This release adds support for dynamically-loadable modules, through the *elf2dyn* command-line utility and the libdyn target library. For details, refer to the online help.

Building Multi-Core Loader Files

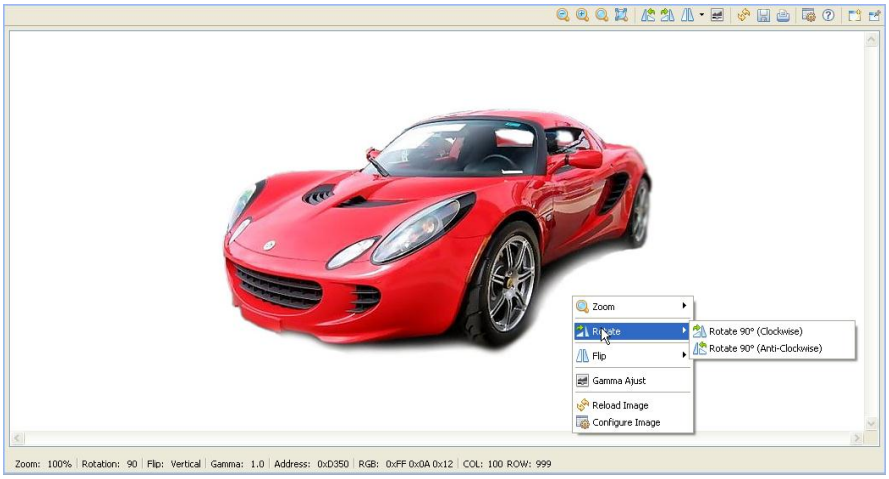
This release provides an extension to the -NoFinalTag switch in the Blackfin loader for better control in combining multiple DXE files to a single ldr file. The -NoFinalTag can now be scoped to specific DXE files. For details, refer to the online help in the ADSP-BF60x Processor Loader Guide section in the Loader and Utilities manual.

Migrating VisualDSP++ files to CrossCore Embedded Studio

This release extends the functionality provided by the elf2elf migration utility, to include migration of .OVL files (for overlays) and .SM files (for VisualDSP++ projects that used SHARED_MEMORY). elf2elf now also includes a -merge switch that can combine such additional files into the main .DXE file. For further details, refer to the online help.

Image Viewer

A new debug view known as the Image Viewer has been added to this release. This view acts much like a memory window, however it allows you to view the contents of memory as an image in any number of configurable input formats. This is especially useful when debugging imaging applications where data is being retrieved from a camera and then processed.



Eclipse 3.7.2

The version of Eclipse upon which the IDE has been built has been upgraded to version 3.7.2. More information on the changes in this release of Eclipse can be found here:

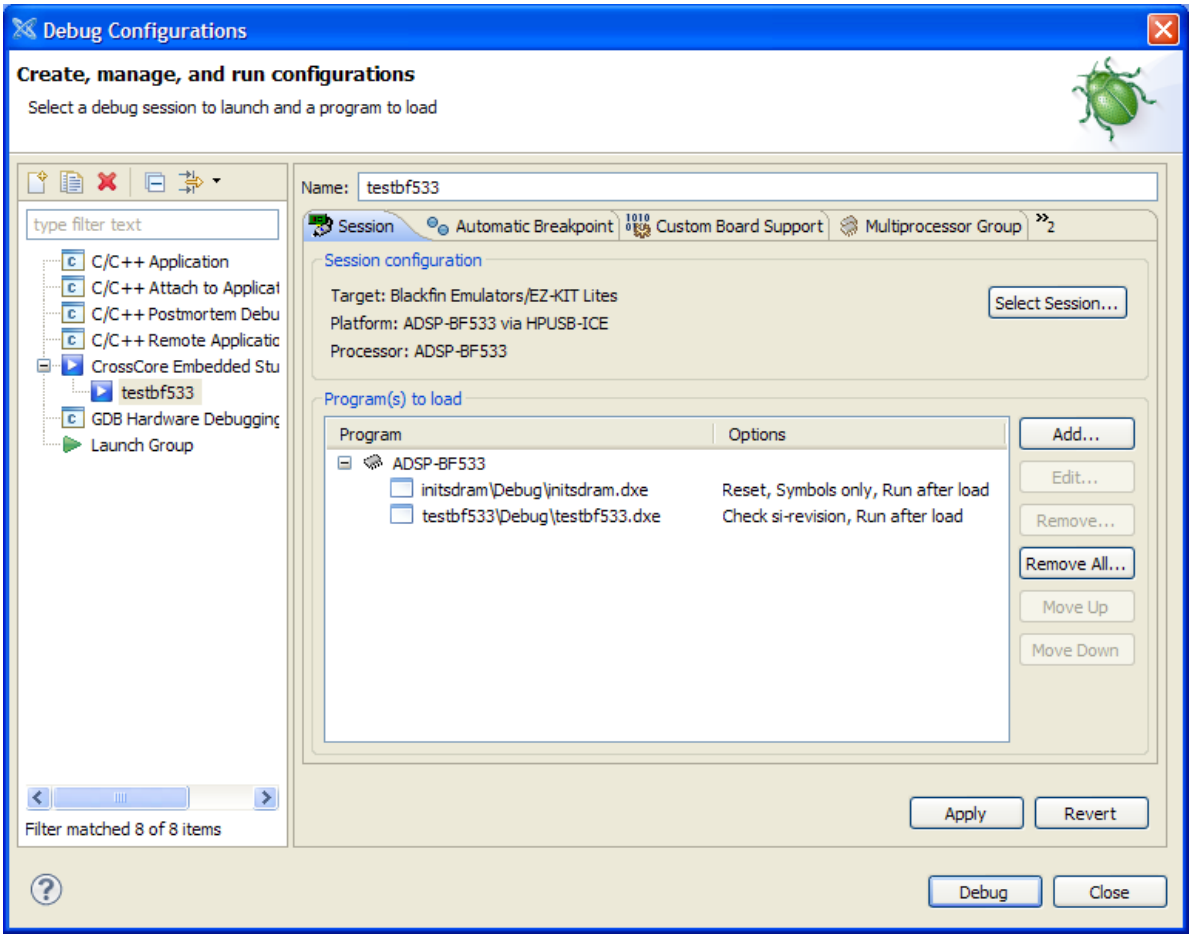
- Eclipse 3.7.2 Release Notes

Bugs and enhancements addressed in this release can be found here:

- Issues addressed in Eclipse 3.7.2 and CDT 8.0.2

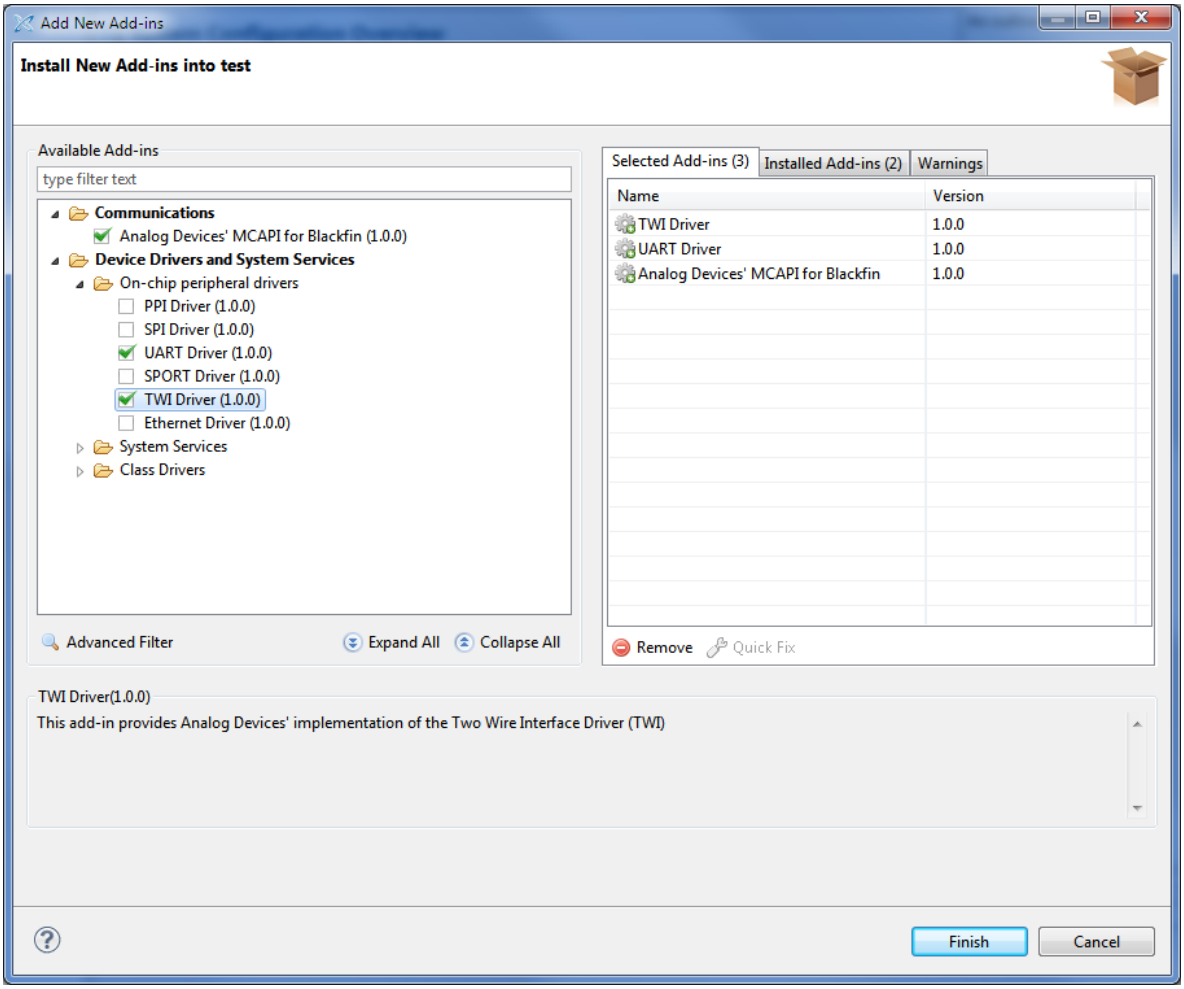
Application Loading Enhancements

In this release the Launch Configuration dialog has been enhanced to allow users to load multiple dxes at the same time with the option to merge symbols, perform resets or load symbols only on each application listed. This is useful for developing applications that are spread across multiple dxe files (say one for a ROM image and another for the standard application).



Add-in Wizard Enhancements

The overall look and feel of the Add-in page in the System Configuration Editor and the New Project Wizard has been enhanced to provide better usability as well as more helpful diagnostics when add-in conflicts are detected.



Linker Support for External Memory

The CCES 1.0.1 linker has support for external memory for the SHARC processors ADSP-2136[7-9], ADSP-2137[1,5], ADSP-2146[7,9], ADSP-2147[7-9], ADSP-2148[3,6-9] as follows:

(1) Synchronous external memory (e.g., DDR2) and asynchronous external memory (e.g., flash) are distinguished by specification of the keywords SYNCHRONOUS and ASYNCHRONOUS in the TYPE specification of the LDF MEMORY statement. If neither is specified for an external memory region the linker assumes the region is SYNCHRONOUS. Note that all default LDFs supplied with CCES 1.0.1 have been modified to specify these keywords.

(2) The linker xml files in $CCESDir\System\ArchDef defining the valid external memory ranges allow specification of the synchronicity (attributes synchronous and asynchronous) and memory bank (attribute bank). Here $CCESDir denotes the CCES 1.0.1 installation directory. e.g., C:\Analog Devices\CrossCore Embedded Studio 1.0.1

(3) The linker performs logical to physical address translation before comparing external memory regions in the LDF for overlap; omission of this translation could cause overlaps to be missed or non-overlapping regions to be reported as overlapping.
The linker translates the logical address specified in the LDF to the external memory physical address as follows:

External Memory Data

All accesses to external memory data must use normal word (i.e., 32 bit) addressing. The mapping of logical address (L) to physical address P in a bank beginning at logical address B and for memory width w is:

```
f = 32/w ;
P = (bank == 0) ? f * L  :  B + ( L - B) * f ;
```

External Memory Instructions

The mapping of logical address L to physical address P for instructions (bank 0 only) is dependent on the memory width w and whether the code is VISA or ISA:

```
For ISA code:  P = (48/w) * L
For VISA code: P = (16/w) * L;
```

The impact of these items is that a user-written LDF imported from VisualDSP may cause the CCES 1.0.1 linker to generate errors where none appeared before. As a temporary work-around new external memory overlap errors may be inhibited by specifying the linker option -nomema; this turns off external memory address translation.

To eliminate such errors permanently will require editing of the LDF MEMORY statement for external memory regions: the keyword SYNCHRONOUS or ASYNCHRONOUS should be added and the logical address range amended, if necessary, to be compatible with those specified in the linker xml file for the processor.

Examples usage

The supported method to find and open examples with CrossCore Embedded Studio is via the Example Browser which is included in the release. Examples should also build and run correctly if they are opened in-place with Eclipse's "Import Project" menu. Importing examples with the "Copy To Workspace" tickbox selected may result in examples which do not build and/or run as expected.

Version Compatibility

This is to provide users with information for use in updating an existing application that was developed with the previous version of the product.

Macro Changes for ADSP-BF60x Headers

This release defines macros in the ADSP-BF60x processor headers that correspond to the ADSP-BF60x Blackfin (r) Processor Hardware Reference, Preliminary Revision 0.4, May 2012.

Your code may need changes if it relied on the defBF609.h / cdefBF609.h headers in the CCES 1.0.0 release. The following are the incompatibilities to be aware of:

- **DDR macros are now prefixed as DMC**

  CCES 1.0.0 names were ones such as REG_DDR0_CFG, BITM_DDR_CFG_EXTBANK, ENUM_DDR_CFG_EXTBANK1. With DMC as the prefix, these are now REG_DMC0_CFG, BITM_DMC_CFG_EXTBANK, ENUM_DMC_CFG_EXTBANK1. To upgrade, make the following global edits:

  REG_DDR0_ to REG_DMC0_
  BITP_DDR_ to BITP_DMC_
  BITM_DDR_ to BITM_DMC_
  ENUM_DDR_ to ENUM_DMC_
  PARAM_DDR_ to PARAM_DMC_
  HAS_DDR to HAS_DMC

- **The SDRSIZE4G enumeration for SDRSIZE field in register DDR_CFG is invalid**

  b#-0110 is not a valid mask for the SDRSIZE field in REG_DDR0_CFG / REG_DMC0_CFG. Code using ENUM_DDR_CFG_SDRSIZE4G / ENUM_DMC_CFG_SDRSIZE4G will no longer build because the invalid macro was removed.

- **EMAC**

  The EMAC macros were substantially revised in CCES 1.0.1 from CCES 1.0.0. Consult the defBF60[6789].h headers in the installation and the Ethernet Media Access Controller (EMAC) chapter in the ADSP-BF60x Blackfin®

Processor Hardware Reference on www.analog.com.

- **USB**

  The USB macros were substantially revised in CCES 1.0.1 from CCES 1.0.0. Consult the defBF60[6789].h headers in the installation and the Universal Serial Bus (USB) chapter in the ADSP-BF60x Blackfin® Processor Hardware Reference on www.analog.com.

- **CAN_INT register in CAN module has bit field name changes**

CCES 1.0.1 (new names)	CCES 1.0.0
BITP_CAN_INT_CANRX	BITP_CAN_INT_CANTRX
BITM_CAN_INT_CANRX	BITM_CAN_INT_CANTRX
BITP_CAN_INT_MBRIRQ	BITP_CAN_INT_MBIRQ
BITM_CAN_INT_MBRIRQ	BITM_CAN_INT_MBIRQ

Other Known Issues

Nothing to report.

For the latest anomalies, please consult our Software and Tools Anomaly page (http://www.analog.com/software-anomalies.html). This page will be available in October 2012.