Release Notes for CrossCore Embedded Studio 1.2.0

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1 Introduction

This document describes the changes for CrossCore Embedded Studio (CCES) 1.2.0. This release adds support for ADSP-BF70x silicon revision 1.0.

1.1 Supported Operating Systems

This release of CCES is supported on the following operating systems:

- Windows XP Professional SP3 (32-bit only)
- Windows Vista Business, Enterprise, or Ultimate SP2 (32-bit only)
- Windows 7 Professional, Enterprise, or Ultimate (32 and 64-bit)
- Windows 8.1 Pro or Enterprise (32 and 64-bit)

> **Note**
>
> Windows Vista, Windows 7, and Windows 8 users may experience User Access Control (UAC) related errors if the software is installed into a protected location, such as `Program Files` or `Program Files (x86)`. We recommend installing the software in a non-UAC-protected location.

1.2 System Requirements

Verify that your PC has these minimum requirements for the CCES installation:

- 2 GHz single core processor; 3.3GHz dual core or better recommended
- 1 GB RAM; 4GB or more recommended
- 2 GB available disk space
- One open USB port

> **Note**
>
> A faster disk drive decreases the build time, especially for a large amount of source files. 4GB of RAM or more will substantially increase the performance of the IDE.

2 New Functionality

2.1 ADSP-BF70x silicon revision 1.0 added

ADSP-BF70x silicon revision 1.0 is supported in CCES 1.2.0, in addition to silicon revision 0.0. Silicon revision 1.0 includes a number of significant silicon fixes including:

- Improved booting functionality.
- Support for misaligned data accesses.
- Corrections to LUT, MSI and Pinmuxing.
- Corrections to the Branch Target Buffer.
- An updated Utility ROM

2.1.1 ADSP-BF70x 1.0 Resolves Secure Boot Fill Block Anomaly 19000022

Secure Boot No Longer Requires LDR File With No Fill Blocks

ADSP-BF70x processors support Secure Booting, where the loader stream is digitally signed and /or encrypted using the signtool utility, and the processor's Boot Kernel decrypts the stream and authenticates the signature before permitting the stream to boot.

ADSP-BF707 silicon revision 1.0 fixes secure boot anomaly 19000022. This anomaly described a problem in silicon revision 0.0 that related to processing "fill blocks" when booting in secure mode, which caused the boot to fail. To avoid the problem, loader streams for silicon revision 0.0 require the elfloader's -NoFillBlock switch. As of silicon revision 1.0, it is no longer necessary to add -NoFillBlock to the elfloader build for secure boot.

There is no problem processing "fill blocks" in non-secure mode, for either silicon revision 0.0 or silicon revision 1.0.

2.1.2 Utility ROM Improvements for ADSP-BF70x revision 1.0

Silicon revision 1.0 of ADSP-BF70x processors includes the following updates to the Utility ROM:

- The libdsp/libcc/libc components have been further optimized for the Blackfin+ core.
- C/OS-III has been updated to use version 3.04.04 of Micrium's product.
- LIBDRV was updated to add new drivers for RSI and HADC peripherals.

A new set of libraries, LDF symbol maps, include files and DXE files for simulation debugging have been included in CCES 1.2.0 to support using the ADSP-BF70x parts silicon revision 1.0 utility ROM.

Warning

Before running an executable on an ADSP-BF70x processor, ensure that the executable has been built for the correct silicon revision:

- Applications that use the utility ROM and are built for 0.0 silicon will not function correctly on 1.0 silicon.
- Applications that use the utility ROM and are built for 1.0 silicon will not function correctly on 0.0 silicon.
- Applications that do not use the utility ROM, or are built for revisions *any* or *none* are unaffected by this update to the utility ROM.

2.1.3 Run-Time Library support for ADSP-BF70x revision 1.0

A new version of the libraries (linked against when building for silicon revision 1.0) is provided which omits workarounds for anomalies that are no longer present in silicon revision 1.0. These anomalies are:

- 19000018 : L1 Parity Checking Detects Spurious Parity Errors
- 19000019 : Misaligned Accesses to L2 or L3 Memory Return Incorrect Data
- 19000042 : Self-Nested Interrupts Disable Further Interrupts
- 19000044 : Dynamic Branch Prediction for RTS Instructions May Cause Data Loss

Refer to the anomaly documentation for further information. Support for existing anomalies is unchanged.

2.2 Branch Target Buffer Performance Tuning

The startup code for ADSP-BF70x processors uses an improved default configuration for the Branch Predictor (BP), which shows a gain in performance over a number of benchmarks. There may be specific cases where this revised BP configuration does not perform as well as previously. In such cases, the previous configuration can be restored, or a more appropriate setting used.

Your startup source, system/startup_ldf/app_startup.s, may no t be regenerated automatically to include these changes unless you close and reopen the project or modify any of the system.svc Startup/LDF settings once CCES 1.2.0 is installed. If using a custom startup you will need to incorporate the changes manually.

3 Changed Functionality

3.1 PLL Settings for ADSP-BF70x processors

3.1.1 Revised PLL configurations

Previous versions of CCES contained default settings for the PLL (CGU) which did not correspond to a valid configuration. Please refer to the Core and System Clock Operating Conditions table in revision PrD or later of the ADSP-BF70x data sheet for permissible clock settings.

3.1.2 adi_pwr_SetFreq() API

The adi_pwr_SetFreq() function accepts two parameters: core clock and sysclock. This API has a number of limitations, with respect to ADSP-BF70x processors:

- Since the API only accepts two parameters, it is not possible to specify settings for all the clocks.
- In CCES 1.2.0, this API has only been verified for the case where core clock and sysclock are set to their maximum values of 400MHz and 200MHz, respectively; other permutations have not been verified.

For ADSP-BF70x processors, ADI recommends use of the other APIs in the *Dynamic Power Management Service*. For more details, please refer to the System Run-Time Documentation in the Online Help.