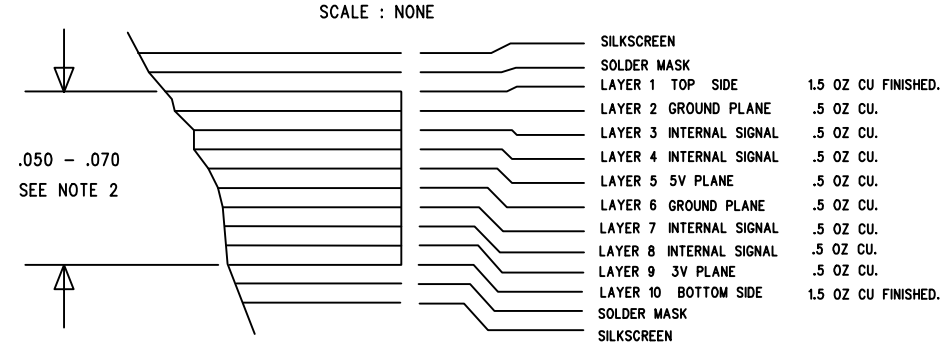
REVISIONS				
REV	DESCRIPTION OF CHANGE	DRFTR	DATE	APPROVED
1.0	NEW RELEASE	C.C.D.	03/06/07	
1.1	REFER TO ECO2007-020	C.C.D.	06/05/07	
1.2	REFER TO ECO2007-044	C.C.D.	06/22/07	
1.3	REFER TO ECO2007-059	C.C.D.	08/16/07	
1.4	REFER TO ECO2007-094	C.C.D.	10/10/07	
2.0	REFER TO ECO2008-091	C.C.D.	11/17/08	

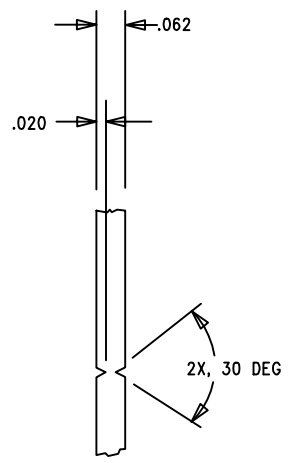
UNLESS OTHERWISE SPECIFIED

1. BOARD TO BE FABRICATED PER IPC-6012A, CLASS 2.
2. MATERIAL: POLYCLAD FR-370HR OR EQUIVALENT. OUTER LAYERS 1/2 OZ/SQFT CU INNER LAYERS 1/2 OZ/SQFT CU FINISHED .062 (.050 MIN .070 MAX SEE DETAIL). VENDOR MAY ADJUST THICKNESS TO FULFILL NOTE 9.
3. PLATING: ADDITIONAL CU PLATING 1 OZ/SQFT ALL HOLES PLATED THROUGH, EXCEPT AS NOTED IN HOLE LEGEND. MINIMUM PTH BARREL THICKNESS = 0.0008" MINIMUM AVERAGE PER IPC-6012A WITH AMENDMENT 1, CLASS 2 REQUIREMENTS. WITH NO SINGLE MEASUREMENT LESS THAN 0.00071 IN THE PLATED HOLES.
4. FINISH: SURFACES TO BE COATED BY ENIG OF 2 TO 10 MICROINCHES OVER A MINIMUM OF 60-200 MICROINCHES OF LOW STRESS NICKEL.
5. SOLDERMASK: SOLDER MASK TO BE TRANSPARENT GREEN LPI BOTH SIDES PER GERBER FILES.
6. SILKSCREEN: WHITE EPOXY INK, APPLY TO BOTH SIDES PER GERBER FILES.
7. ARTWORK: MINIMUM FEATURE SIZE = 0.00492 MINIMUM AIR GAP = 0.00449
8. ALL DIMENSIONS ARE IN INCHES.
9. CONTROLLED IMPEDANCE: BOARD TO BE BUILT TO YIELD CONTROLLED IMPEDANCE OF 60 OHMS +/-10% (SINGLE ENDED) ON ALL .005" LINE WIDTHS. ALL .007" LINE WIDTHS TO BE 50 OHMS SINGLE ENDED AND 100 OHMS DIFFERENTIAL +/-10%. ALL .0079" LINE WIDTHS TO BE 45 OHMS SINGLE ENDED AND 90 OHMS DIFFERENTIAL +/-10%.
10. DO NOT ADD NON-FUNCTIONAL COPPER THIEVING ON OPEN AREAS OF OUTER LAYERS. THIEVING IS ALLOWED ON INNER LAYERS, UNLESS OTHERWISE SPECIFIED.
11. VIAS SHOULD BE COVERED ACCORDING TO ONE OF THE FOLLOWING METHODS. METHOD 1 IS PREFERRED.
    METHOD 1: VIAS MUST BE FILLED WITH SOLDERMASK MATERIAL AFTER ELECTROLESS NICKEL/IMMERSION GOLD AND BEFORE PRIMARY LPI MASK. AFTER THE FILL IS CURED, THE PRIMARY MASK IS THEN APPLIED WITH NO VIA APERATURES BOTH SIDES.

    METHOD 2: AFTER APPLICATION OF FULL BODY ELECTROLESS NICKEL/ IMMERSION GOLD, APPLY PRIMARY MASK WITH REDUCED VIA APERTURES THAT ARE 6 MILS LARGER THAN DRILLED HOLE DIAMETER BOTH SIDES. THEN APPLY SOLDER MASK PLUG ON COMPONENT SIDE.
12. VIA HOLES (.006, .010, .012, & .014) REQUIRE TANGENCY ONLY, INSTEAD OF ANNULAR RING.
13. TEARDROP PADS ARE ACCEPTABLE WHERE NEEDED.
14. REMOVAL OF NON-FUNCTIONAL PADS ON LAYERS 3, 4, 7, AND 8 IS ACCEPTABLE.
15. USE IPC-D-356A NETLIST AS SUPPLIED FOR CHECKING.
16. V SCORE 1 LINE ON BOTH SIDES OF THE BOARD. SEE DETAIL.
17. BUILD AS 1-UP PCB.
18. THE FOLLOWING NETS ARE INTENTIONALLY SHORTED AND RESULT IN IPC NETLIST ERRORS: AT W1 : GND & AGND (LAYER 10)
    AT W3 : GND & PGND (LAYERS 1 & 10)
    AT W4 : GND & PGND2 (LAYERS 1 & 10)
19. HOLES/VIAS IN AREA SHOWN TO BE FILLED AND LEVELED IN AREAS SHOWN WITH NON-CONDUCTIVE PASTE.

10 LAYER CONSTRUCTION DETAIL
SCALE : NONE





SCORING DETAIL

SIZE	QTY	SYM	PLATED	TOL
0.006	407	+	YES	+.003/-.006
0.01	2129	×	YES	+.003/-.010
0.014	1046	⊡	YES	+.003/-.012
0.028	17	◇	YES	+.003/-.014
0.032	5	⧖	YES	+/-0.003
0.037	12	⋈	YES	+/-0.003
0.038	253	A	YES	+/-0.003
0.043	24	B	YES	+/-0.003
0.047	9	C	YES	+/-0.003
0.05	2	D	NO	+/-0.003
0.053	6	E	NO	+/-0.003
0.055	2	F	YES	+/-0.003
0.055	2	G	NO	+/-0.003
0.063	2	H	YES	+/-0.003
0.071 x 0.173	2	J	YES	+/-0.003
0.117	4	K	NO	+/-0.005
0.125	2	L	NO	+/-0.005
0.125	11	M	YES	+/-0.005
0.128	2	N	NO	+/-0.005
0.167	7	P	YES	+/-0.005

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE : .XX +/- .010 .XXX +/- .005	CONTRACT NO.		
	APPROVALS	DATE	
MATERIAL SEE NOTES	DRAWN C.C.D.	11/17/08	
	CHECKED		
FINISH SEE NOTES	ENGINEERING		
	QUALITY		
DO NOT SCALE THIS DRAWING	MANUFACTURING		

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FABRICATION DRAWING
ADSP-BF527 EZ-KIT LITE

SIZE	DWG. NO.	REV.
B	A0208-2006	2.0
SCALE 1 : 1		SHEET 1 OF 1