

A

B

C

D

1

1

2

2

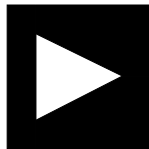
3

3

4

4

ADSP-TS201S EZ-KIT Lite



**ANALOG
DEVICES**

20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title ADSP-TS201S EZ-KIT LITE
TITLE

Size C	Board No. A0178-2002	Rev 2.1C
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Date 6-28-2007_13:24	Sheet 1 of 17
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A

B

C

D

DSP A

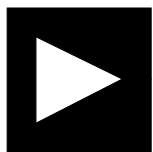
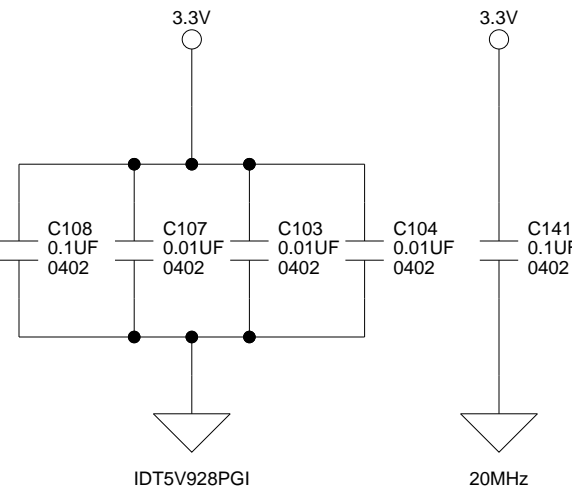
LABEL "DSP A" near this DSP

KEEP THESE NETS THE SAME LENGTH

PLACE CLOSE TO IDT5V928 PINS

PLACE TEST POINTS NEXT TO EACH OTHER

PLACE CLOSE TO EACH OTHER



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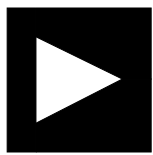
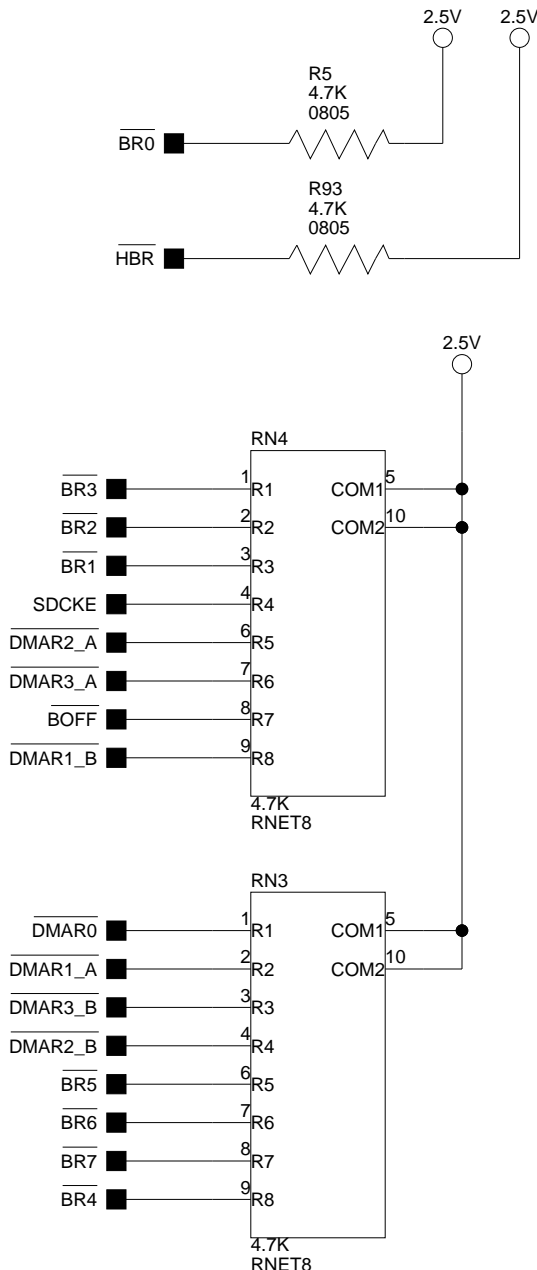
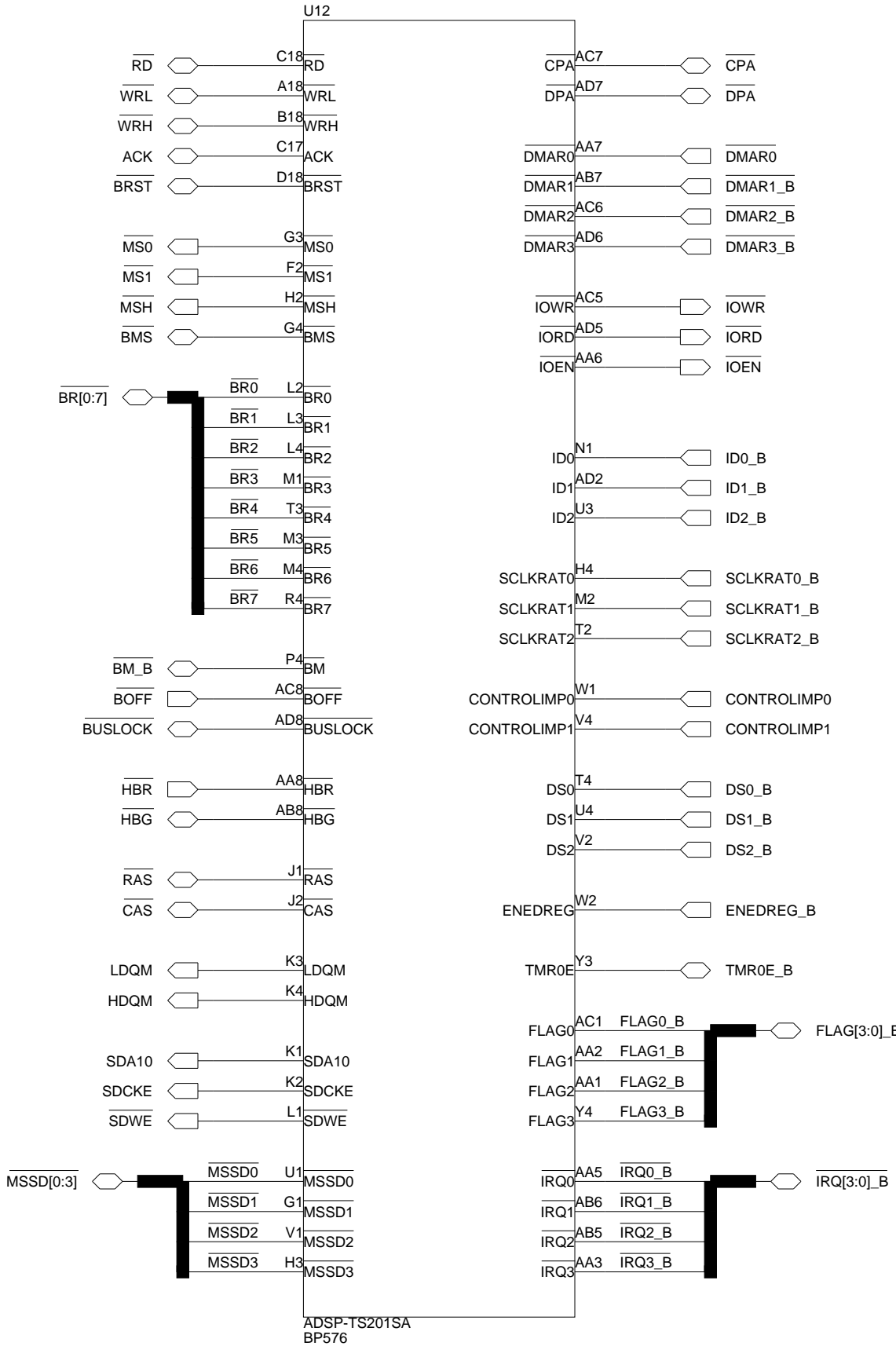
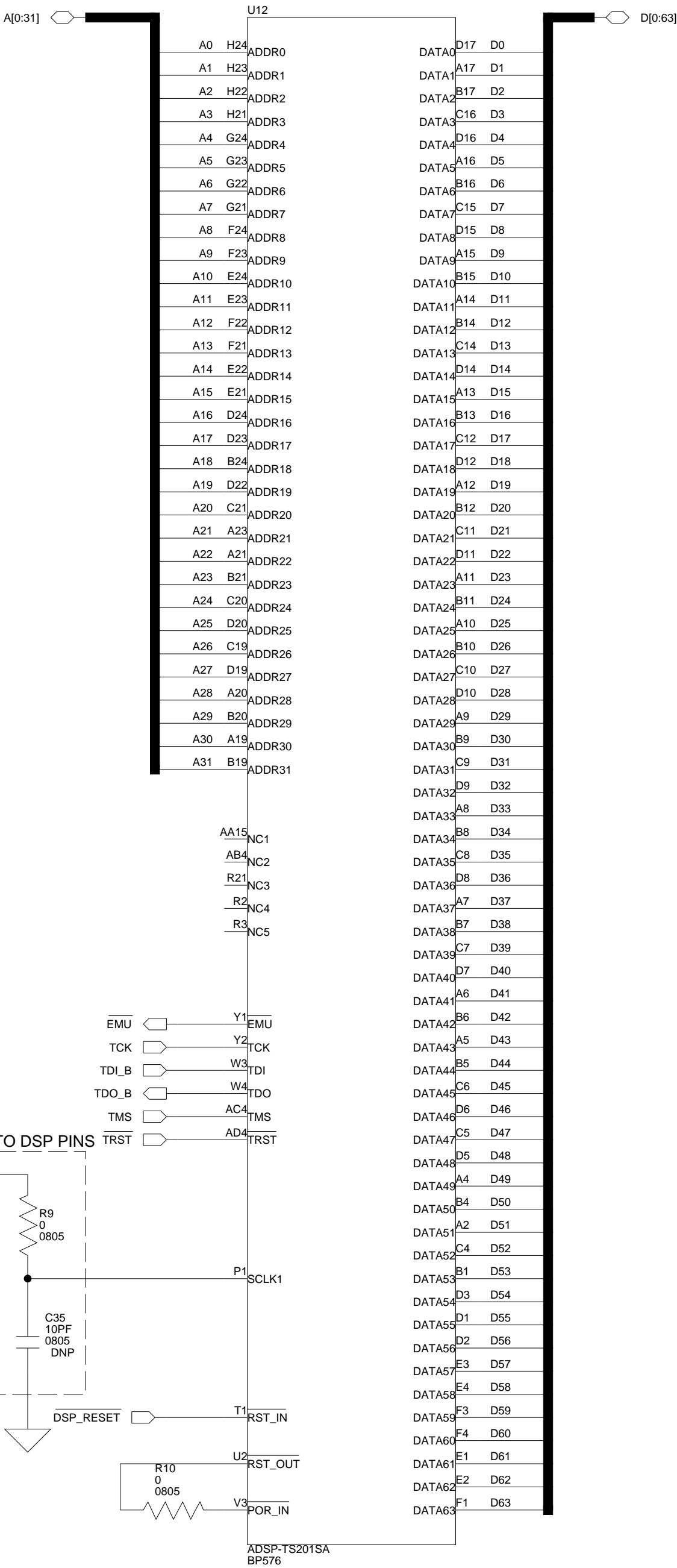
Title **ADSP-TS201S EZ-KIT LITE
DSP A**

Size C	Board No. A0178-2002	Rev 2.1C
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DSP B

LABEL "DSP B" near this DSP



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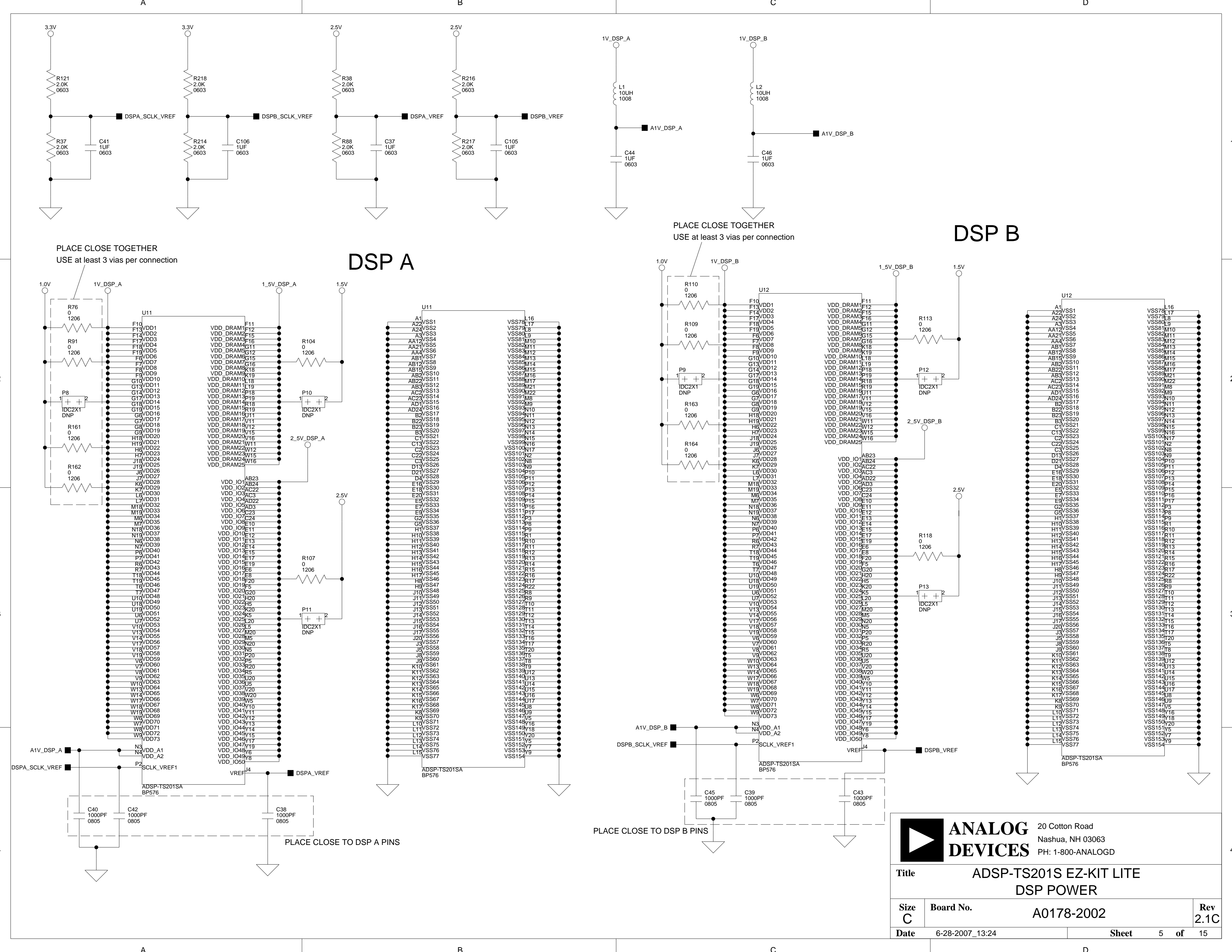
Title **ADSP-TS201S EZ-KIT LITE
DSP B**

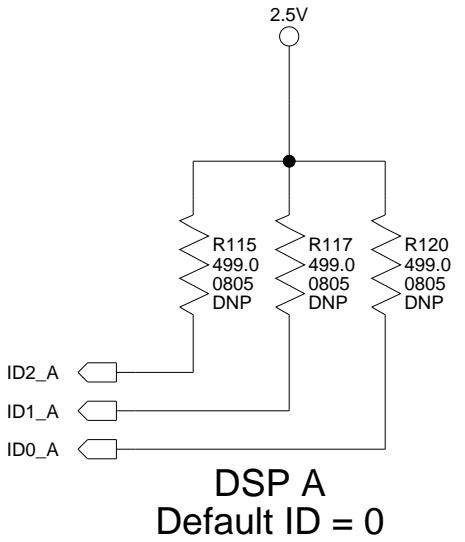
Size **C** Board No. **A0178-2002**

Rev **2.1C**

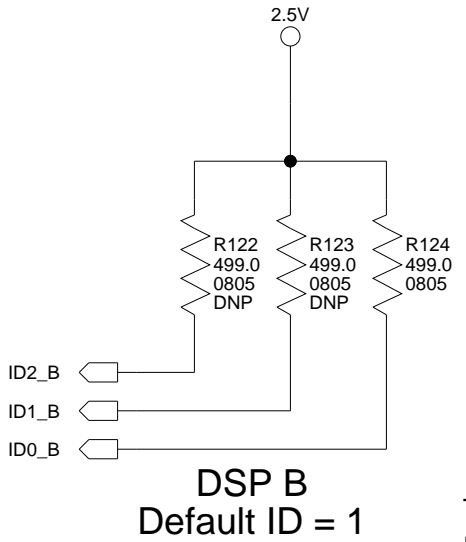
Date 6-28-2007_13:24

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DSP A
Default ID = 0

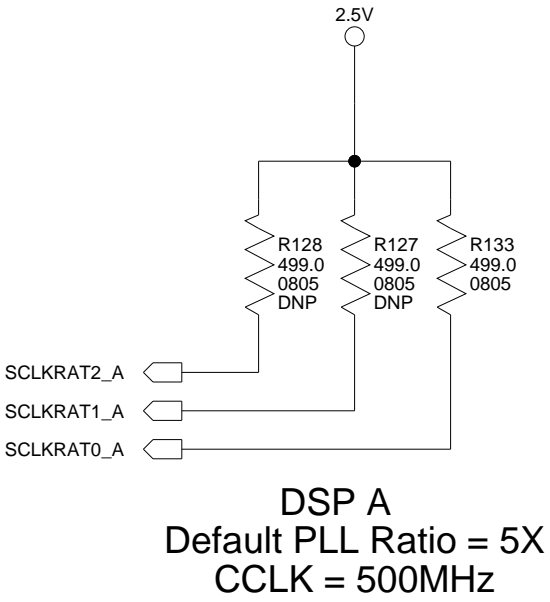


DSP B
Default ID = 1

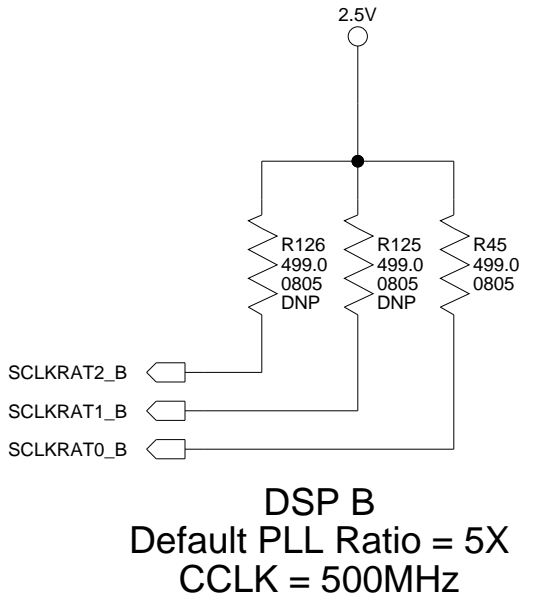
ID[2-0] have internal 5Kohm pull-down resistors

ID(2-0)	Proc ID
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

THESE RESISTORS DO NOT NEED TO BE VERY CLOSE TO THE DSP
IF POSSIBLE I WOULD LIKE THEM ALL ON THE BOTTOM OF THE BOARD
ORGANIZED IN GROUPS SIMILAR TO SHOW HERE
DEPENDING ON HOW MUCH ROOM YOU CAN LEAVE NEAR THEM
I WOULD LIKE TO LABEL SOME OF THEM



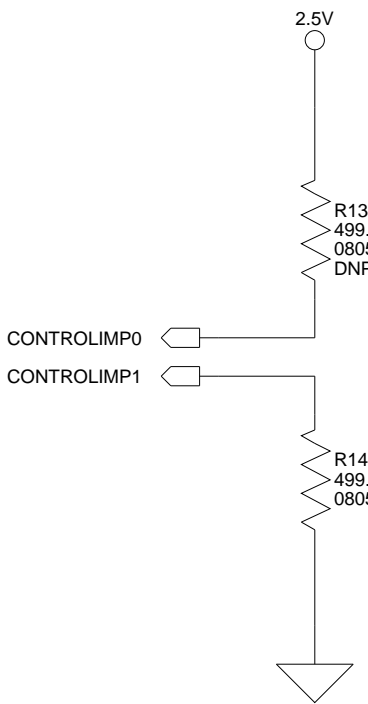
DSP A
Default PLL Ratio = 5X
CCLK = 500MHz



DSP B
Default PLL Ratio = 5X
CCLK = 500MHz

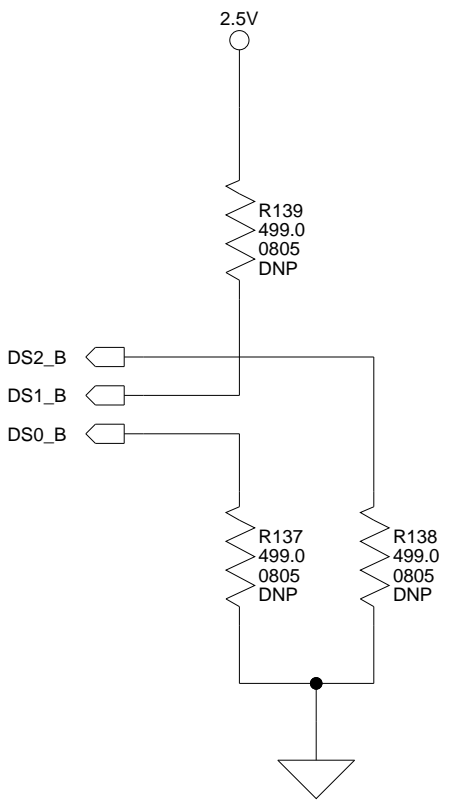
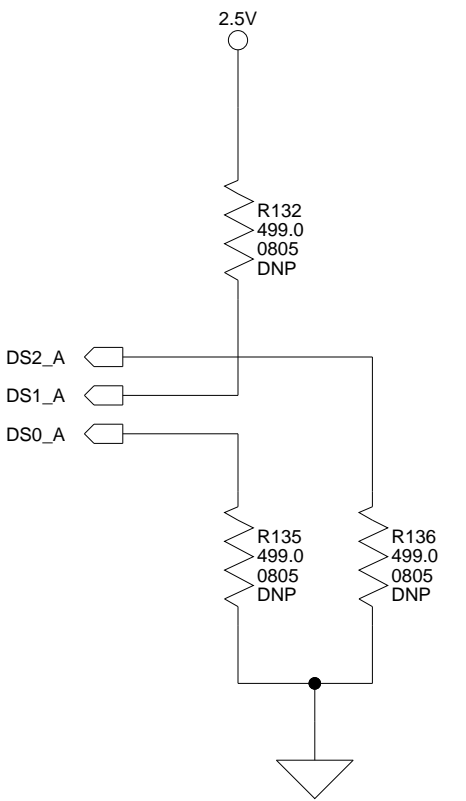
SCLKRAT[2-0] have internal 5Kohm pull-down resistors

SCLKRAT(2-0)	PLL Ratio
000	4
001	5
010	6
011	7
100	8
101	10
110	12
111	RESERVED



DEFAULT = NORMAL
CONTROLIMP0 has an internal 5Kohm pull-down resistor
CONTROLIMP1 has an internal 5Kohm pull-up resistor

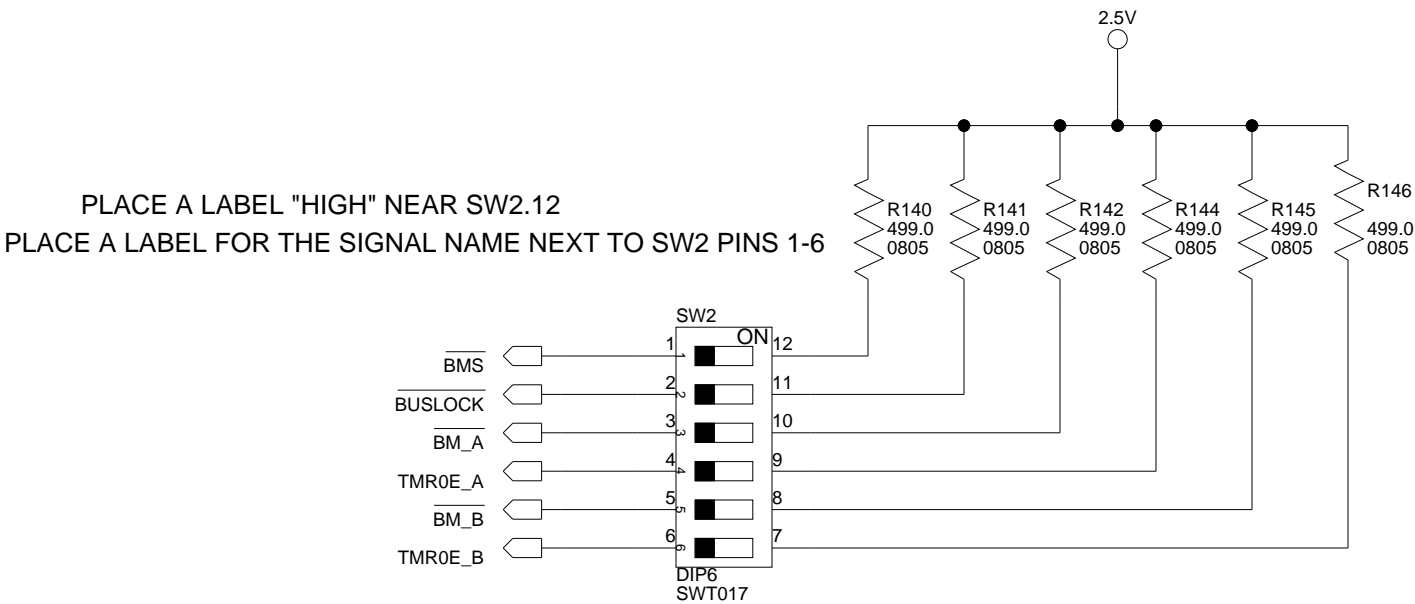
CONTROLIMP(1:0)	Driver Mode
00	Normal
01	Pulse Mode
10	A/D Mode
11	Pulse Mode, A/D Mode



DS1 has internal 5Kohm pull-down resistor
DS2 and DS0 have internal 5Kohm pull-up resistors

DS(2-0)	Drive Strength	OUTPUT IMP
000	11.1%	26
001	23.8%	32
010	36.5%	40
011	49.2%	50
100	61.9%	62
101	74.6%	70
110	87.3%	96
111	100%	120

DEFAULT



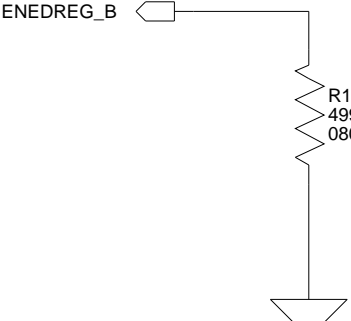
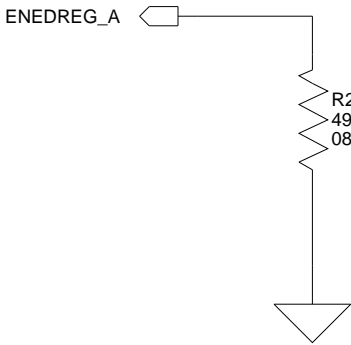
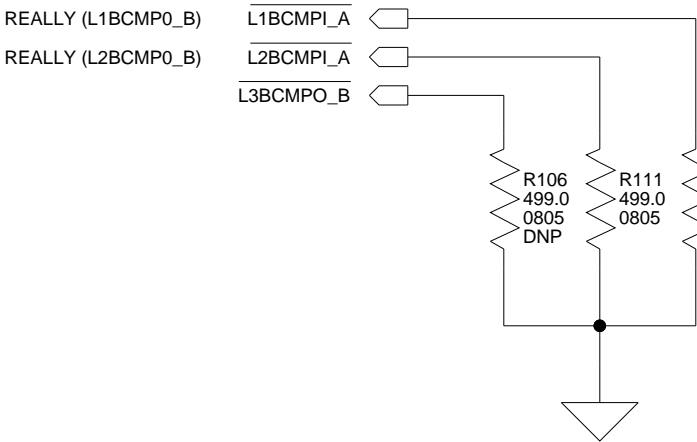
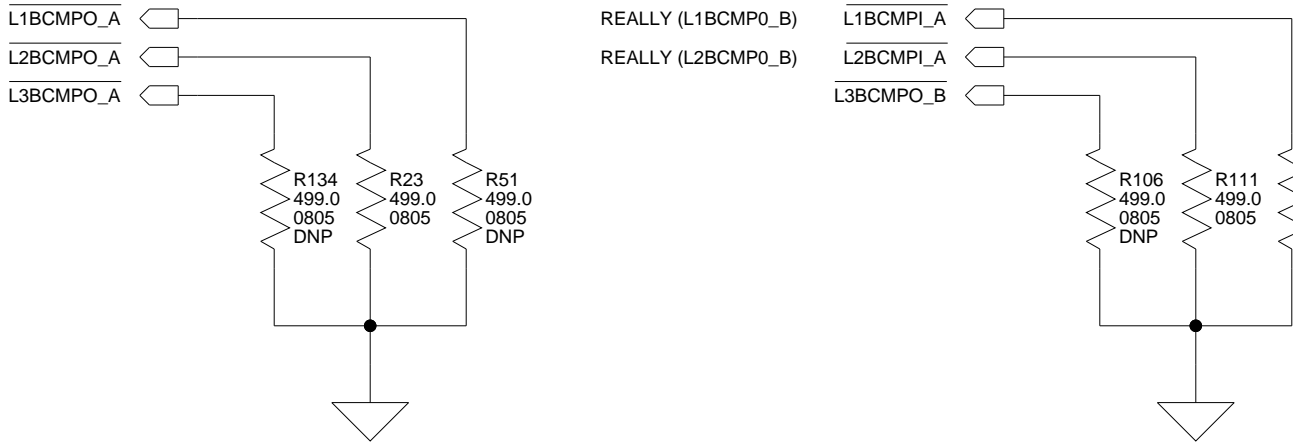
PLACE A LABEL "HIGH" NEAR SW2.12
PLACE A LABEL FOR THE SIGNAL NAME NEXT TO SW2 PINS 1-6

All strap pins have internal 5Kohm pull-down resistors during DSP reset

	Switch OFF (Signal Pulled Low)	Switch ON (Signal Pulled High)
BMS	* EPROM Boot	External or link port boot
BM	* Disable interrupts, level sensitive	Enable interrupts, edge sensitive
TMR0E	* 1-bit Link Port Data Width	4-bit Link Port Data Width
BUSLOCK	* SYSCON/SDRCON one-time writable	SYSCON/SDRCON always writable

* indicates DEFAULT

KEEP STUB TO THE SIGNAL AS SMALL AS POSSIBLE



**ANALOG
DEVICES**

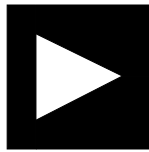
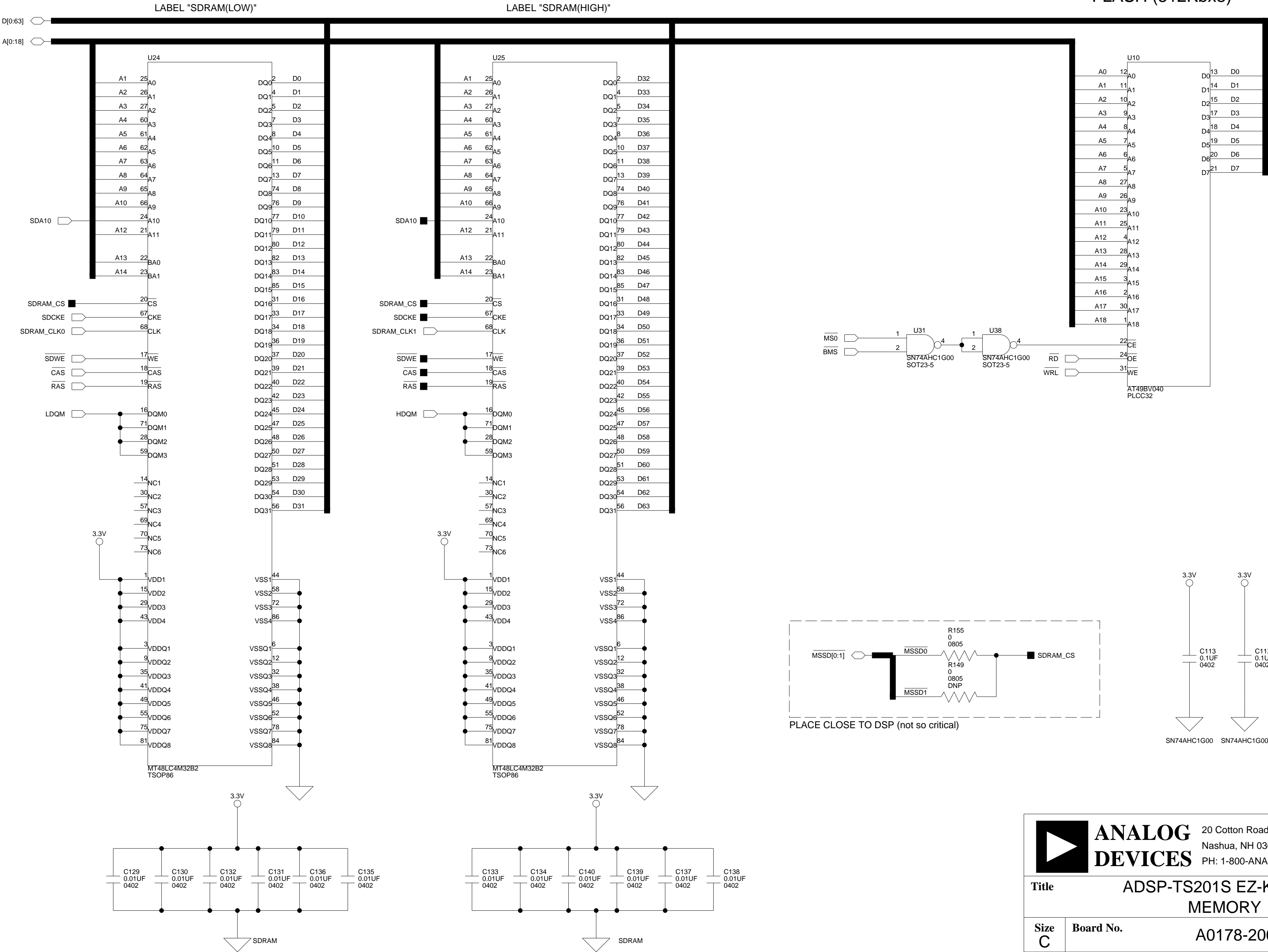
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Nashua, NH 03063
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Title **ADSP-TS201S EZ-KIT LITE
CONFIGURATION**

Size C	Board No.	Rev
	A0178-2002	2.1C
Date	6-28-2007_13:24	Sheet 6 of 15

SDRAM 256Mb
(32MB - 4M x 64bits)

FLASH (512Kbx8)



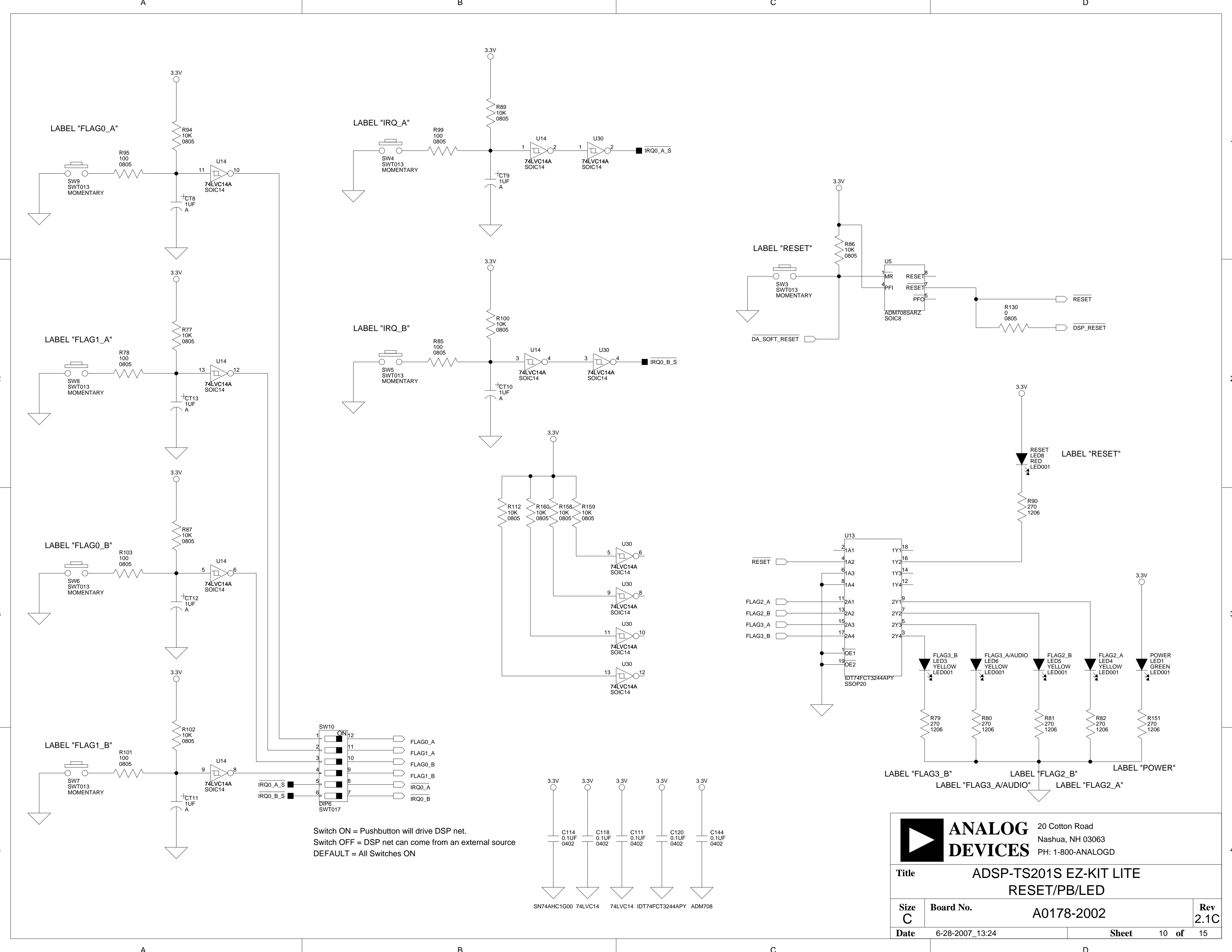
**ANALOG
DEVICES**

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Title **ADSP-TS201S EZ-KIT LITE
MEMORY**

Size C	Board No. A0178-2002	Rev 2.1C
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Title ADSP-TS201S EZ-KIT LITE RESET/PB/LED		
Size C	Board No. A0178-2002	Rev 2.1C
Date 6-28-2007_13:24	Sheet 10 of 15	

Expansion Interface (TYPE A)

PLACE LABEL "EXPANSION INTERFACE (TYPE A)" NEAR MIDDLE CONNECTOR

5V

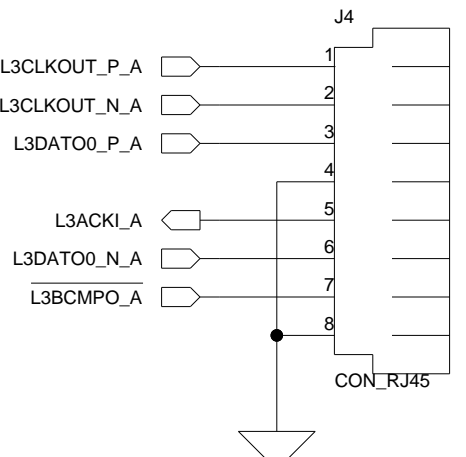
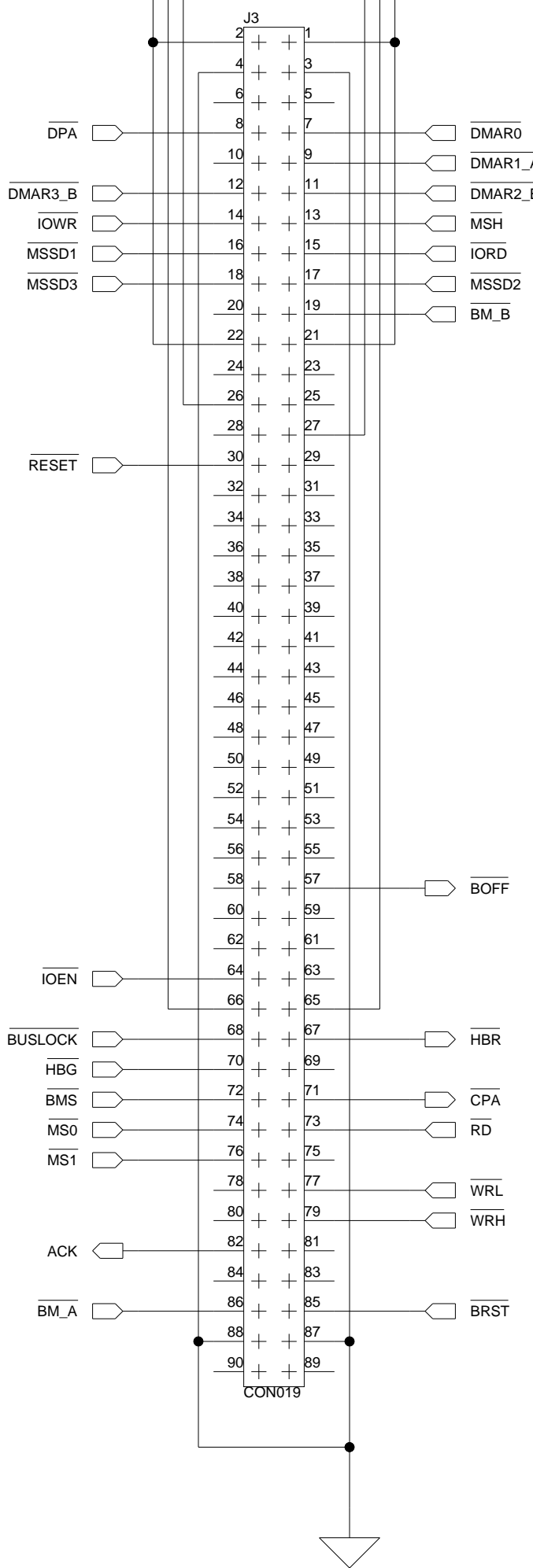
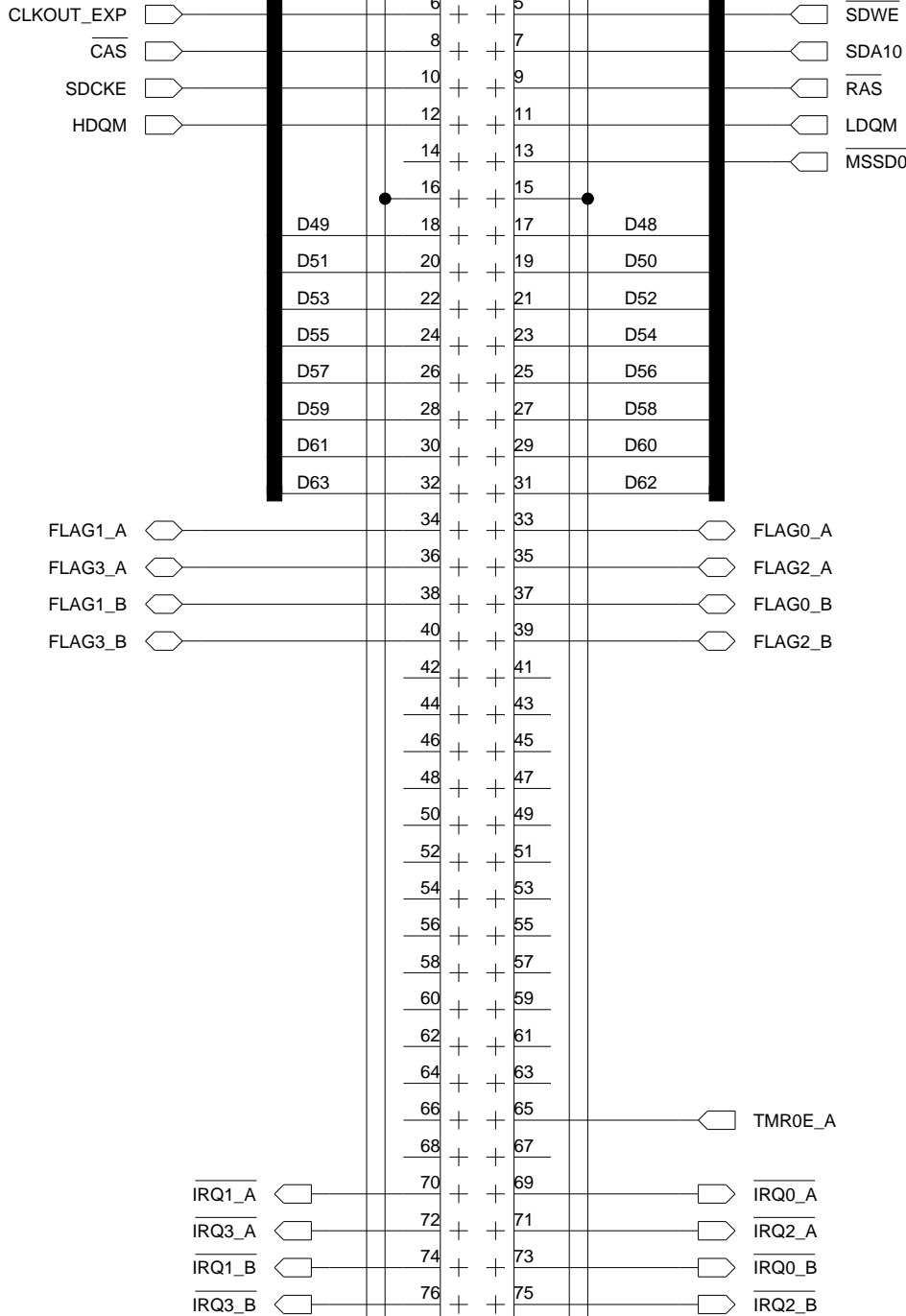
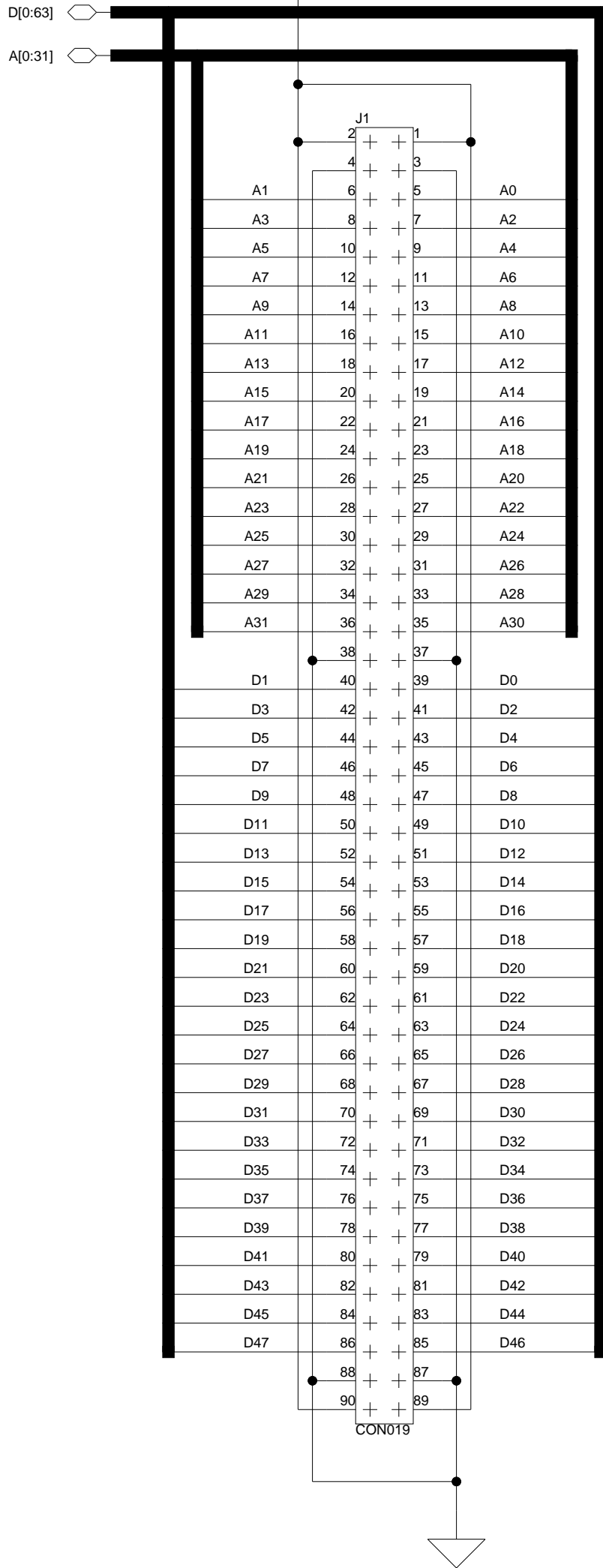
2.5V

2.5V

5V

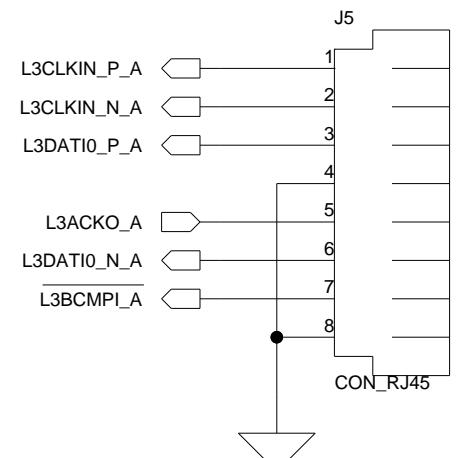
3.3V

WARNING: WHEN CONNECTING TO ANOTHER BOARD
MAKE SURE TX CONNECTOR GOES TO A RX CONNECTOR
DO NOT USE CROSSOVER CABLE



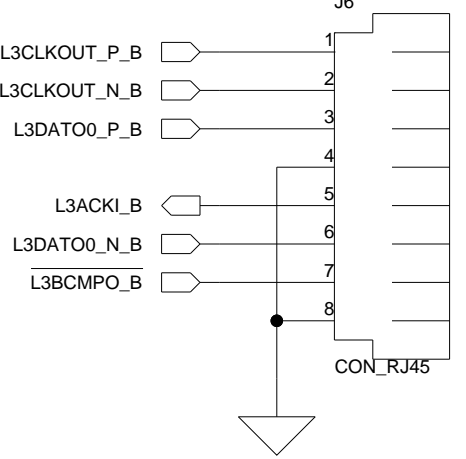
LABEL "DSP A TX"

DSP A TX



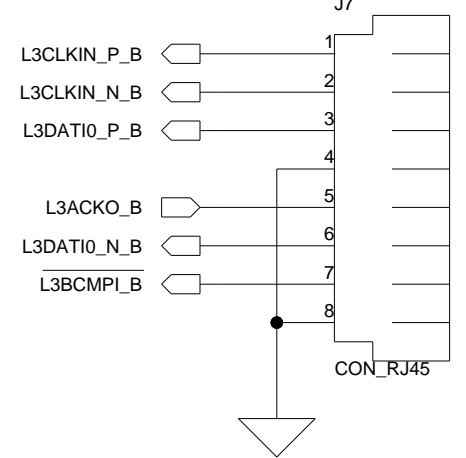
LABEL "DSP A RX"

DSP A RX



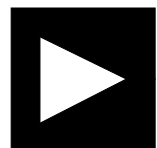
LABEL "DSP B TX"

DSP B TX



LABEL "DSP B RX"

DSP B RX



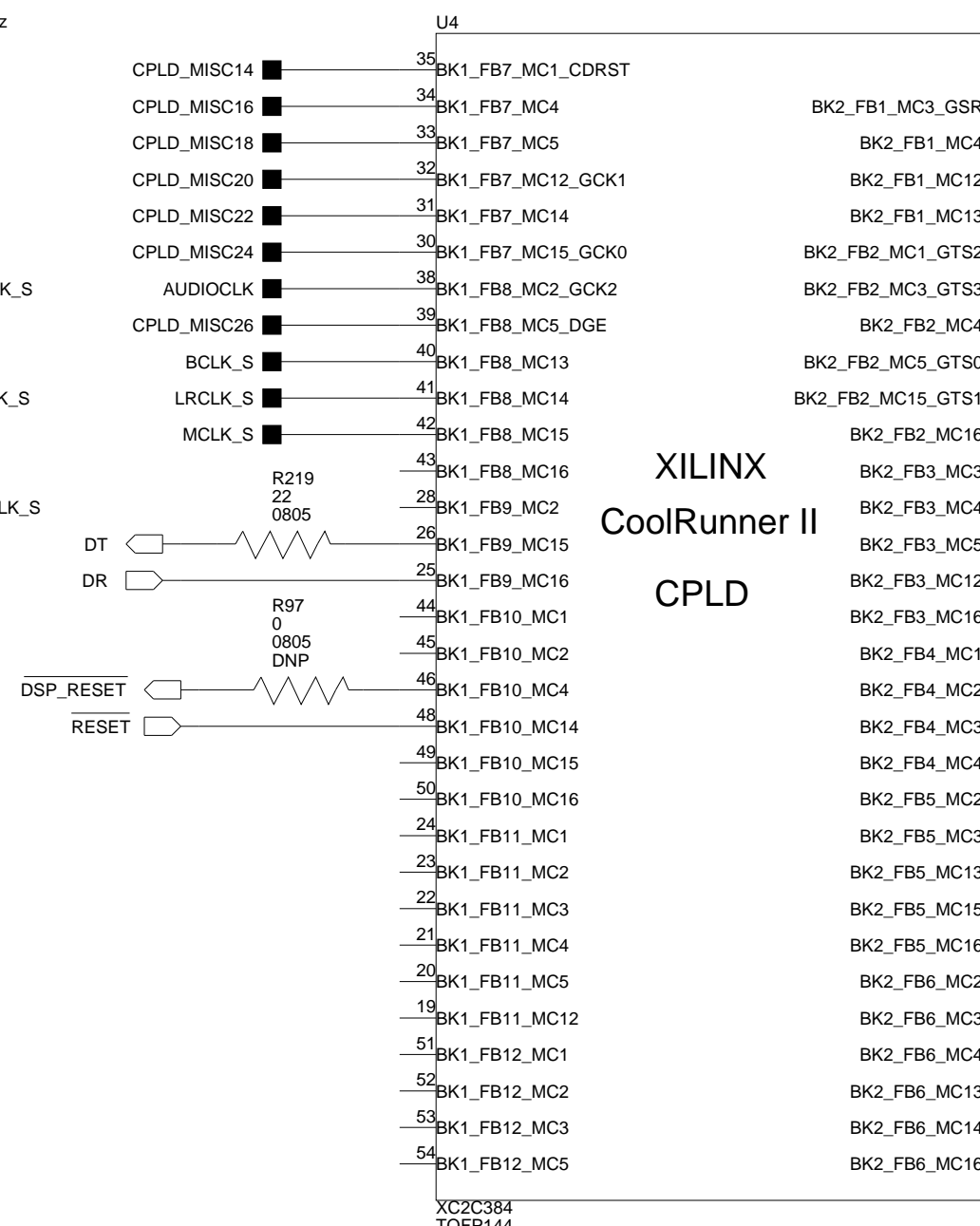
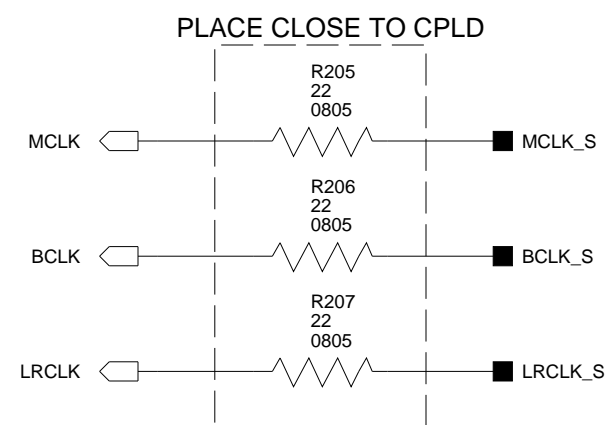
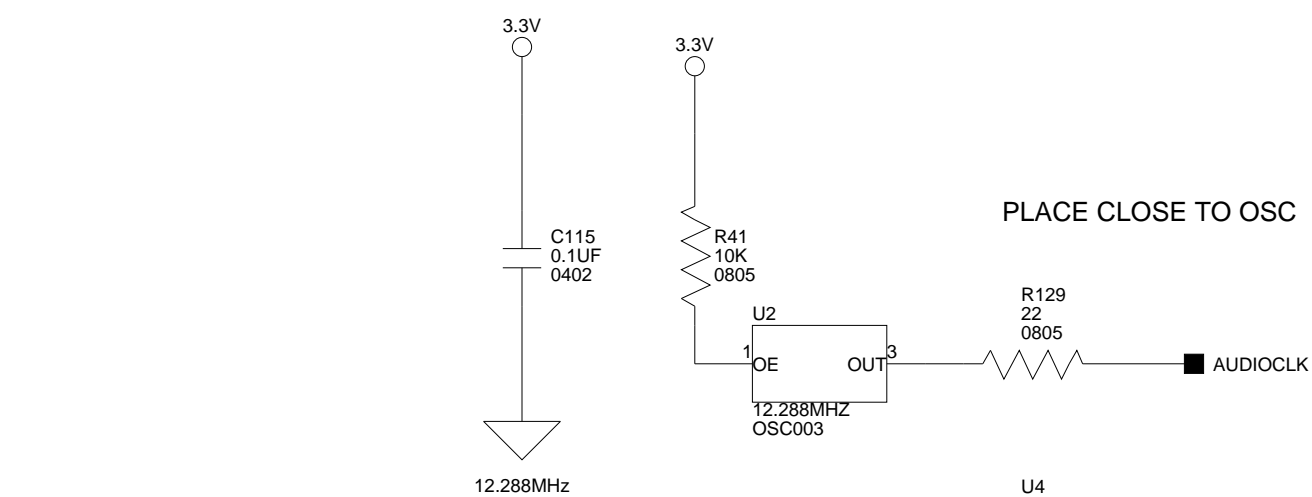
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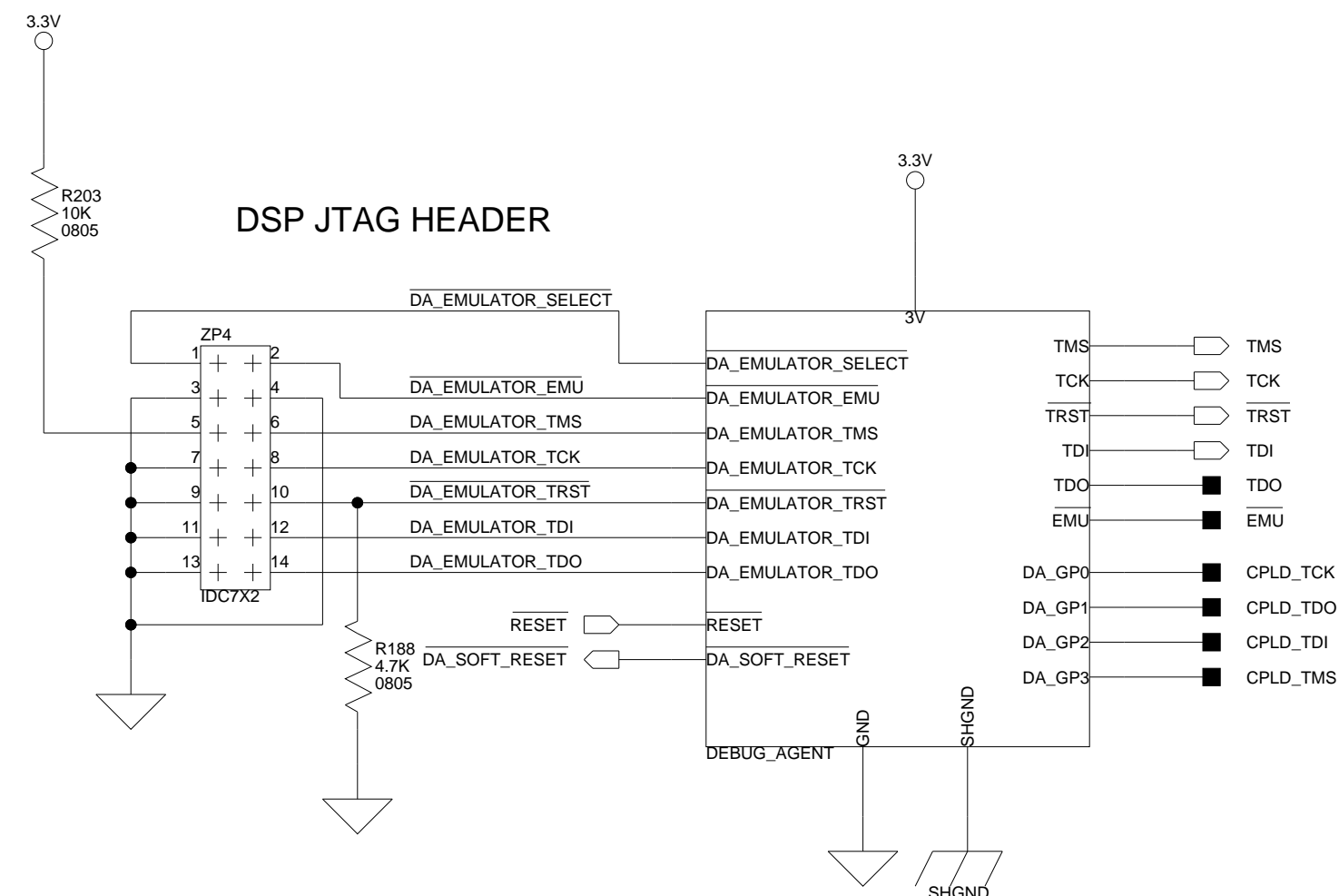
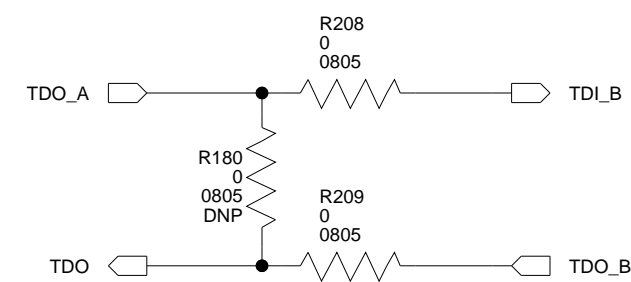
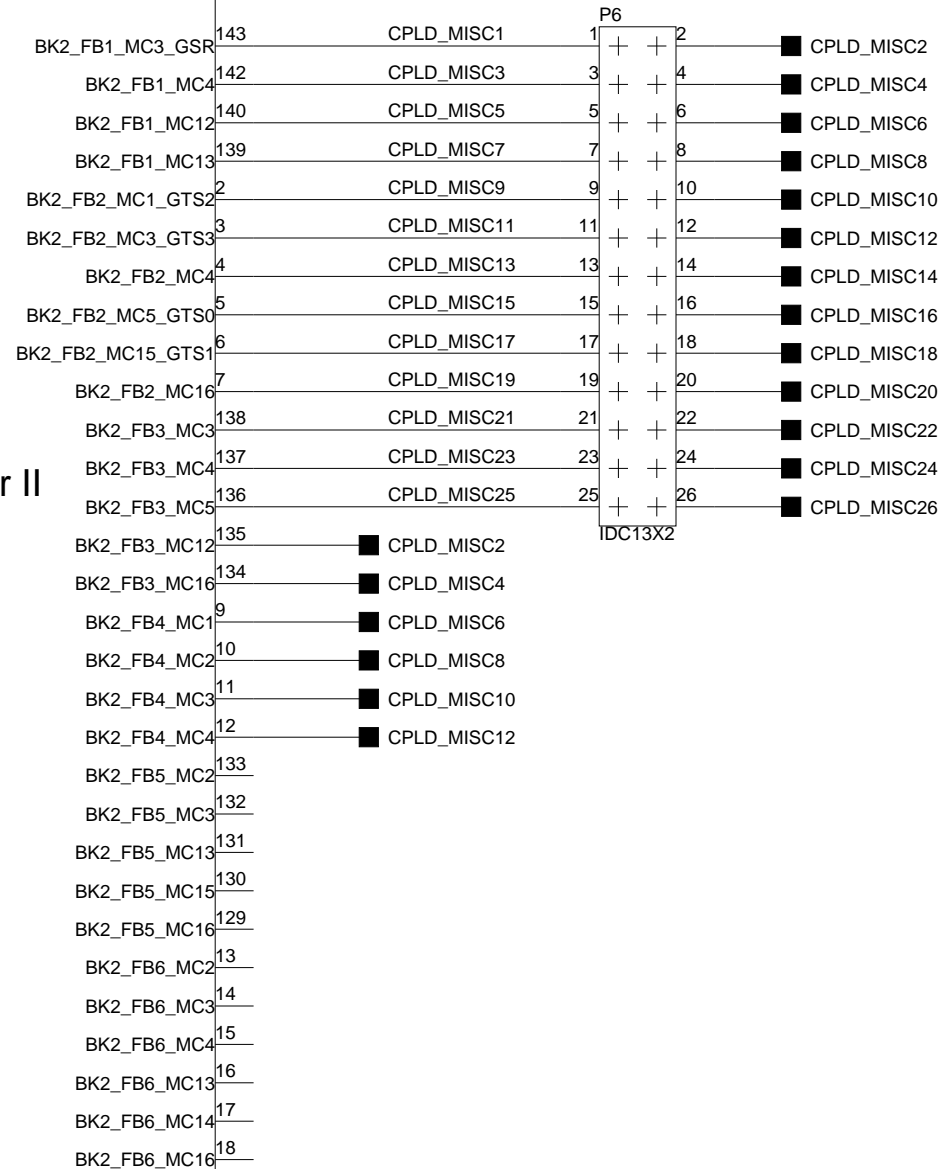
Title ADSP-TS201S EZ-KIT LITE
EXPANSION INTERFACE

Size C Board No. A0178-2002 Rev 2.1C

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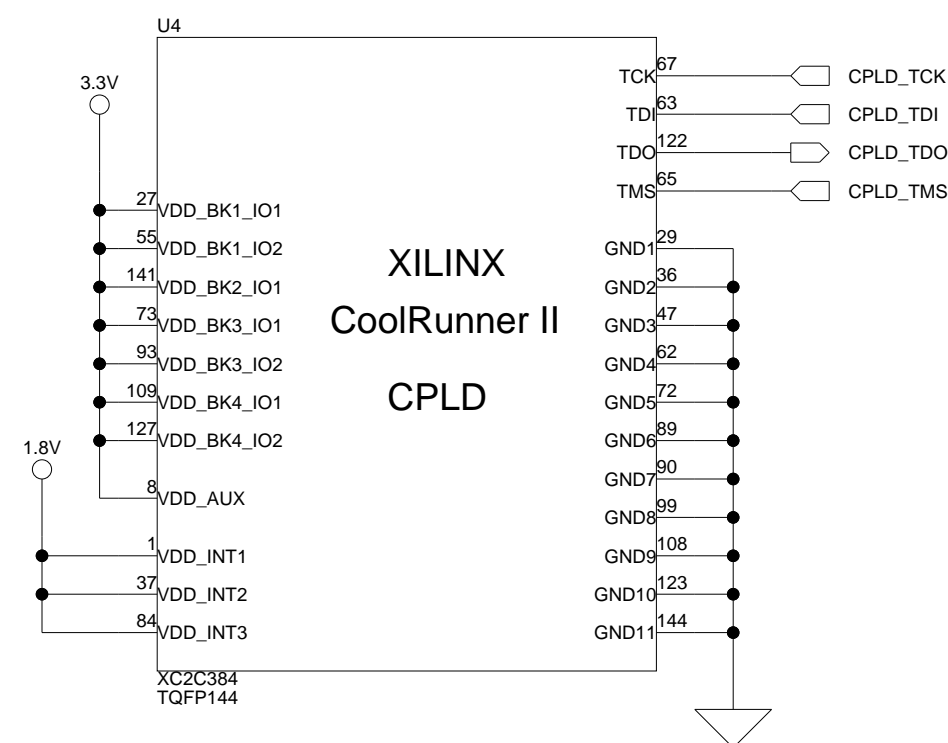


XILINX
CoolRunner II
CPLD

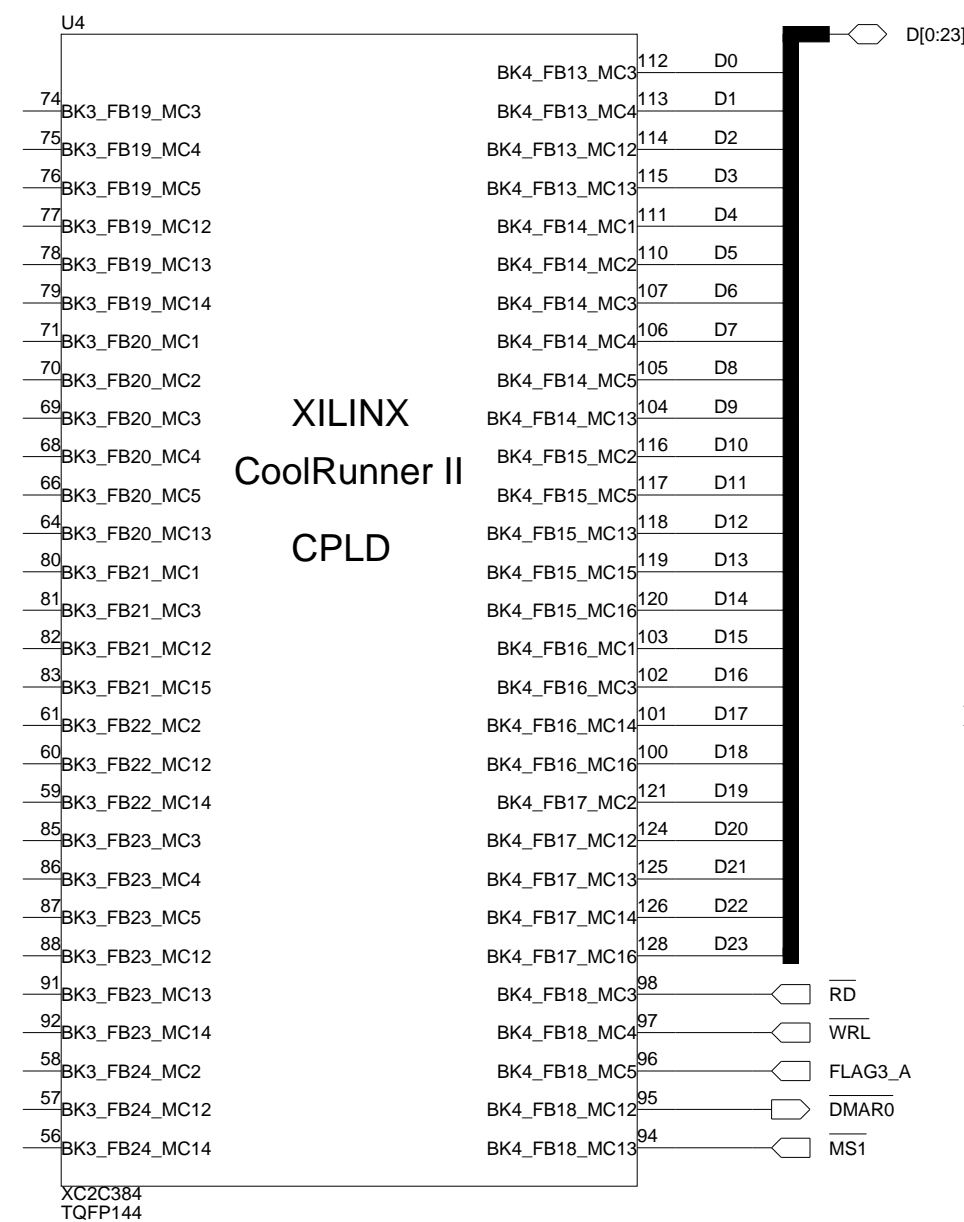


All USB interface is considered proprietary and has been omitted from this schematic.

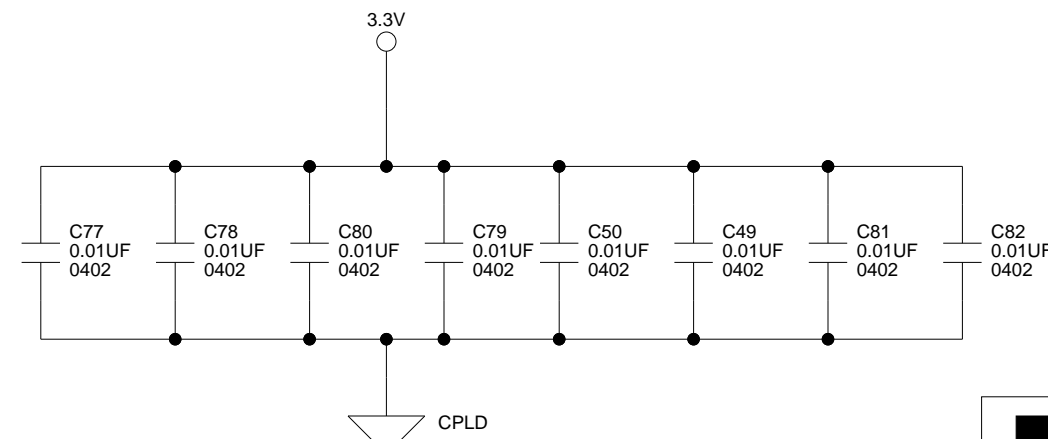
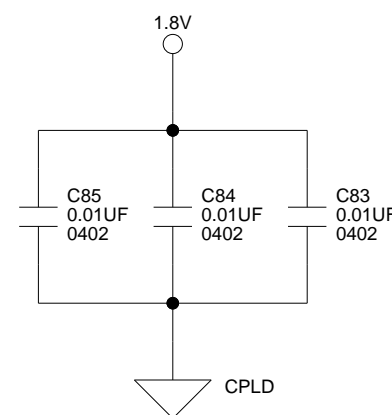
When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at <http://www.analog.com>



XILINX
CoolRunner II
CPLD



XILINX
CoolRunner II
CPLD



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Title **ADSP-TS201S EZ-KIT LITE
JTAG/CPLD FOR AUDIO**

Size
C

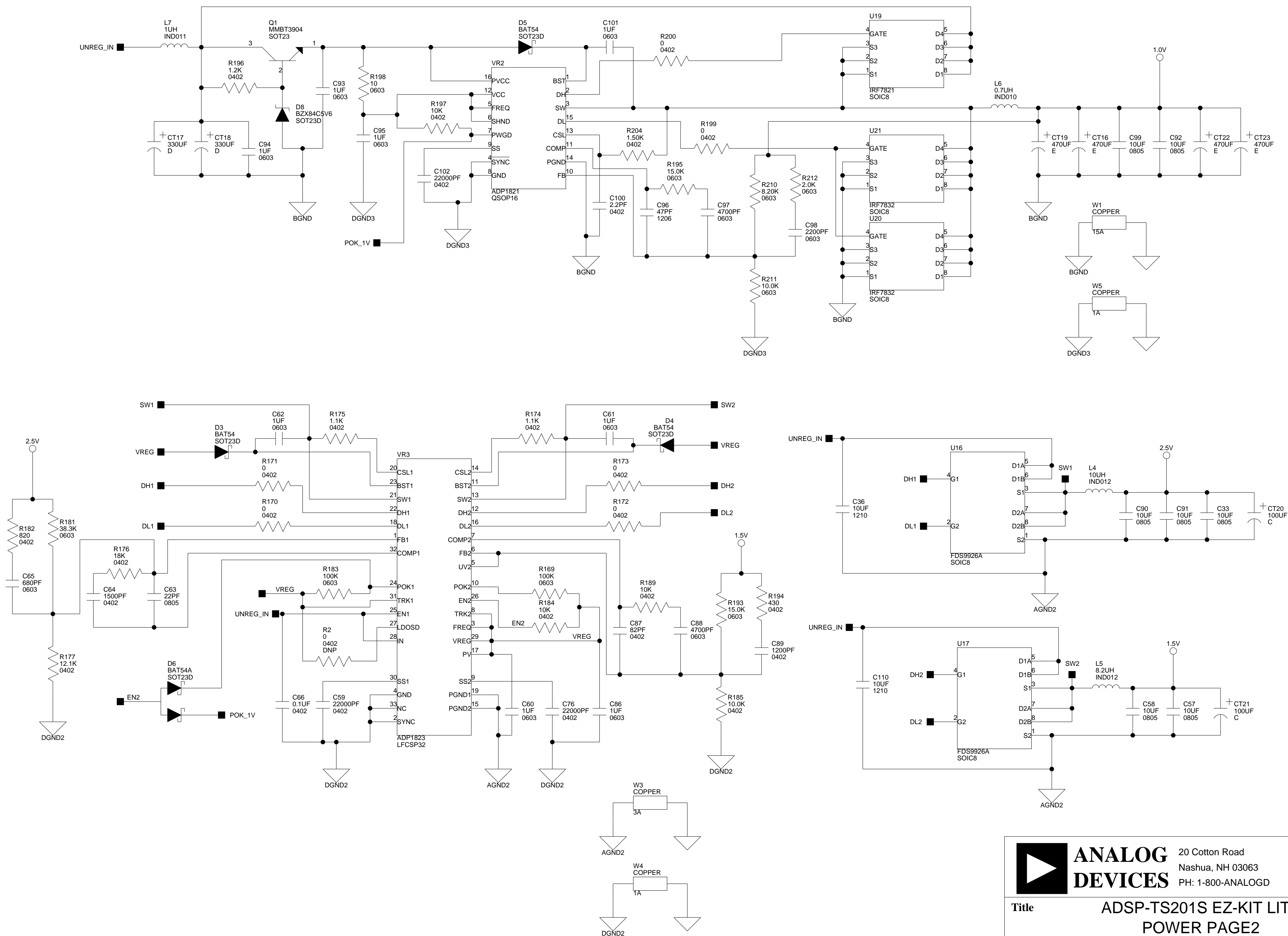
Board No.

A0178-2002

Rev
2.1C

Date 6-28-2007_13:24

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**ANALOG
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PH: 1-800-ANALOGD

Title **ADSP-TS201S EZ-KIT LITE
POWER PAGE2**

Size
C

Board No.

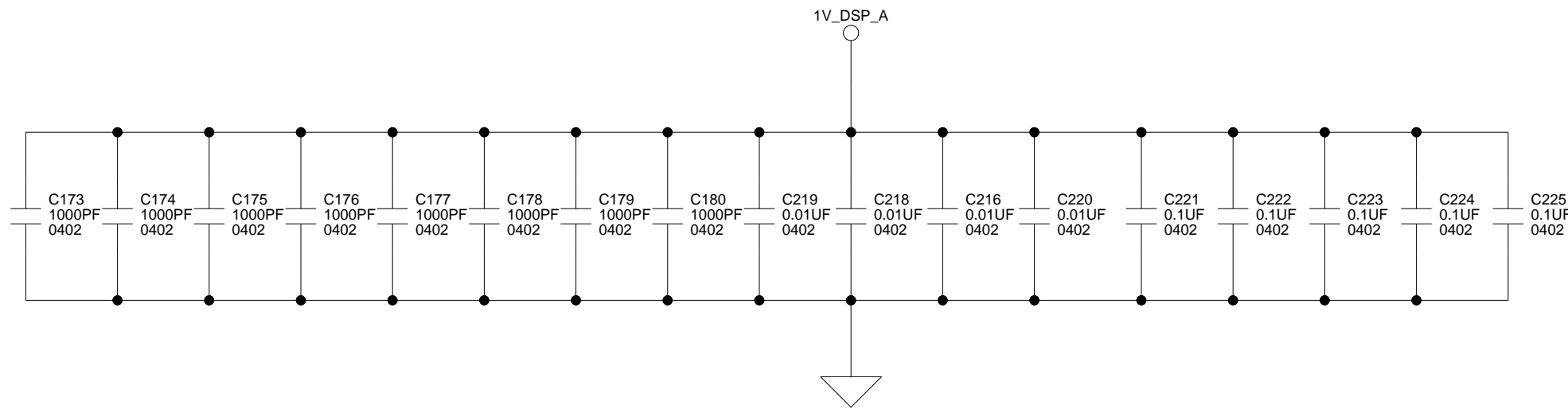
A0178-2002

Rev
2.1C

Date 6-28-2007_13:24

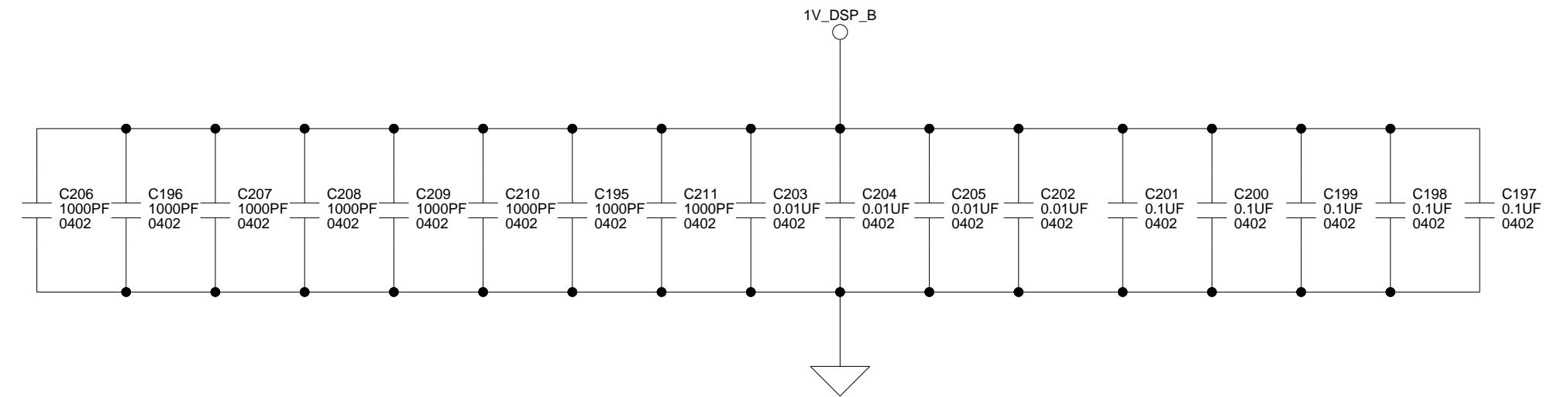
Sheet 14 of 15

VDD (1.0V) Bypass Caps (per DSP)
(8) 1nF
(4) 0.01uF
(5) 0.1uF
(1) 100uF

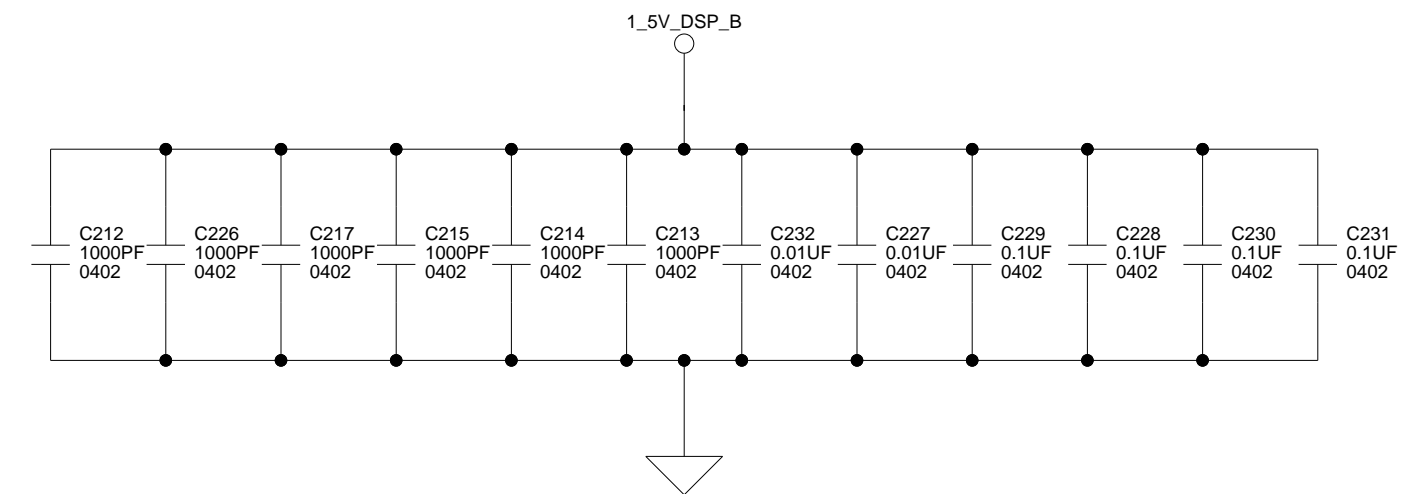
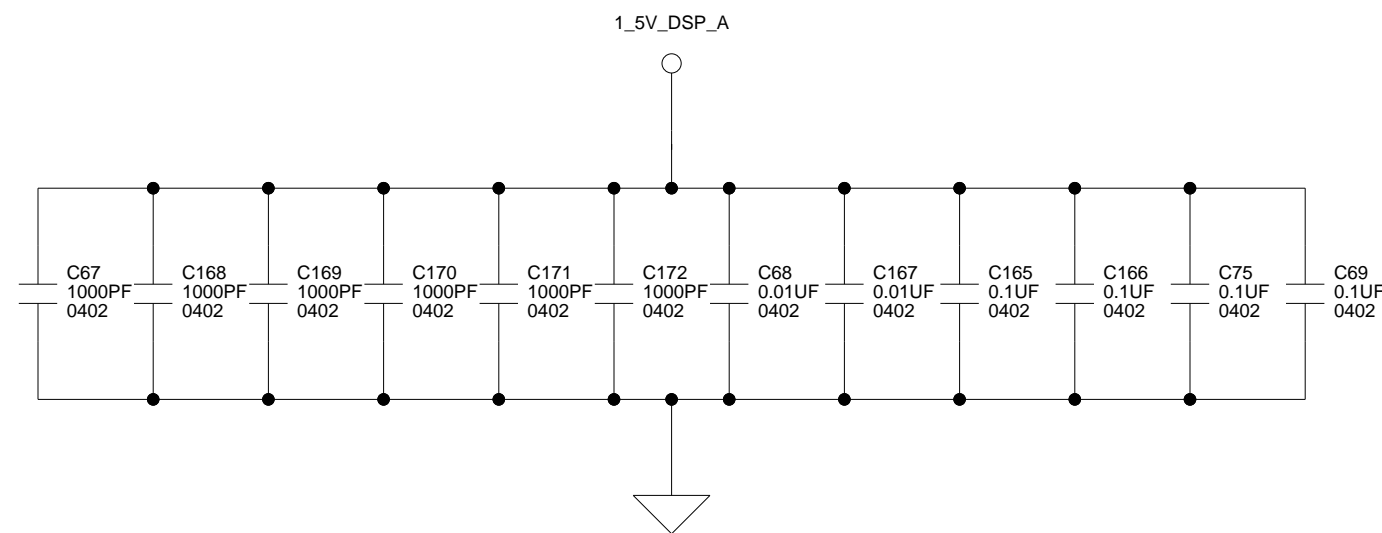


ALL BYPASS CAPS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CORISPONDING IC
TRACES FROM COMPONENT TO CAPACITOR AND FROM THE CAPACITOR TO GND SHOULD BE AS SHORT AS POSSIBLE
THE PRIORITY FOR THE PLACEMENT:

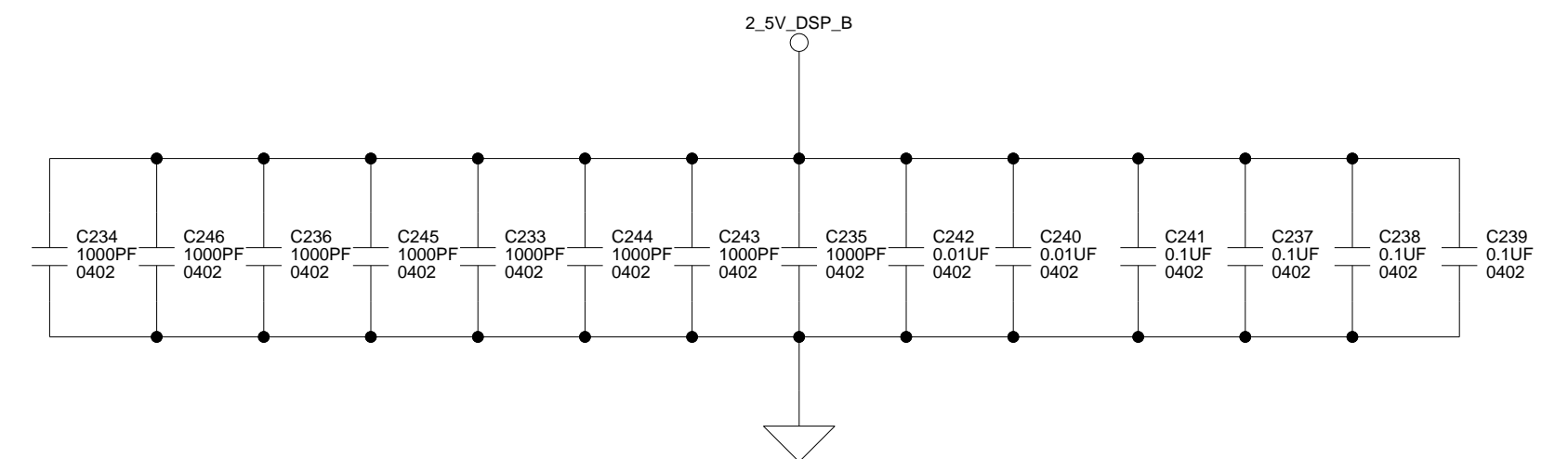
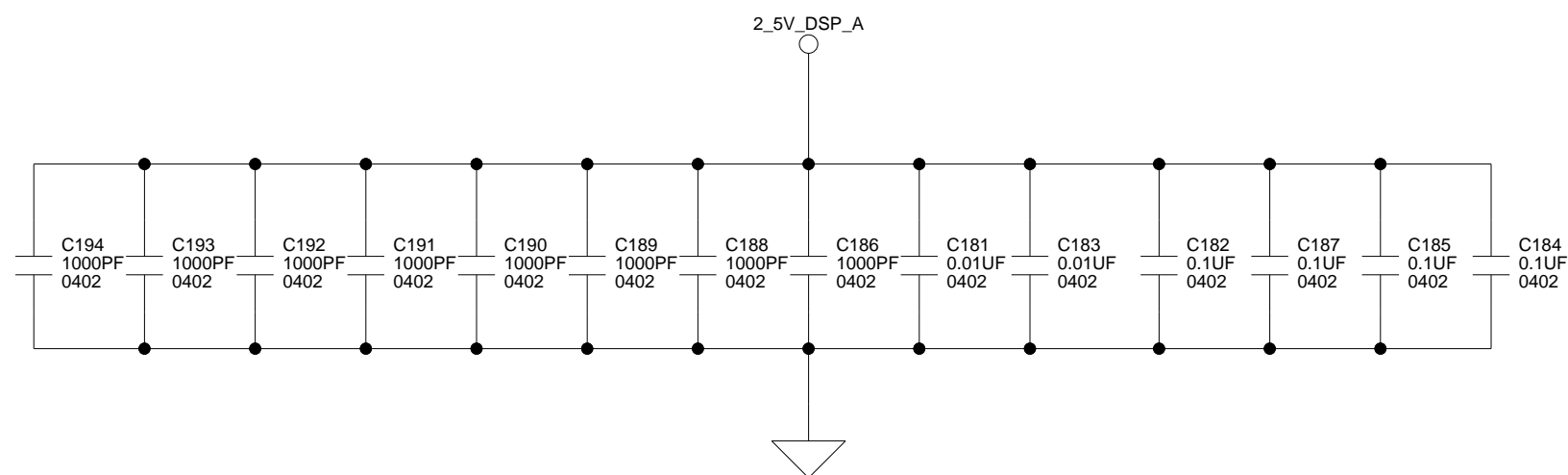
1V_DSP_X
1_5V_DSP_X
2_5V_DSP_X



VDD_DRAM (1.5V) Bypass Caps (per DSP)



VDD_IO (2.5V) Bypass Caps (per DSP)
(8) 1nF
(2) 0.01uF
(4) 0.1uF
(1) 100uF



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Title	ADSP-TS201S EZ-KIT LITE DSP BYPASS CAPS
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Size C	Board No. A0178-2002	Rev 2.1C
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