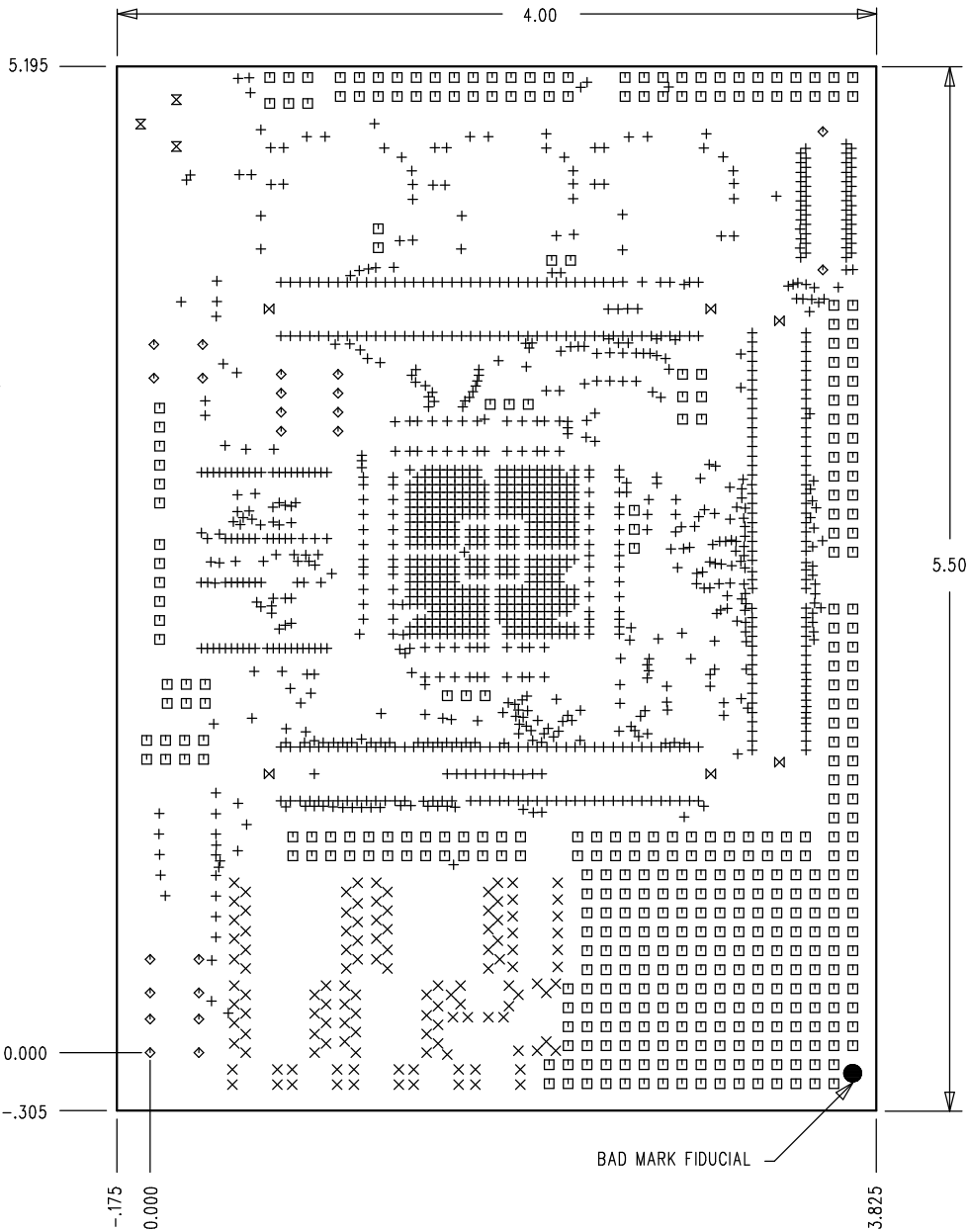
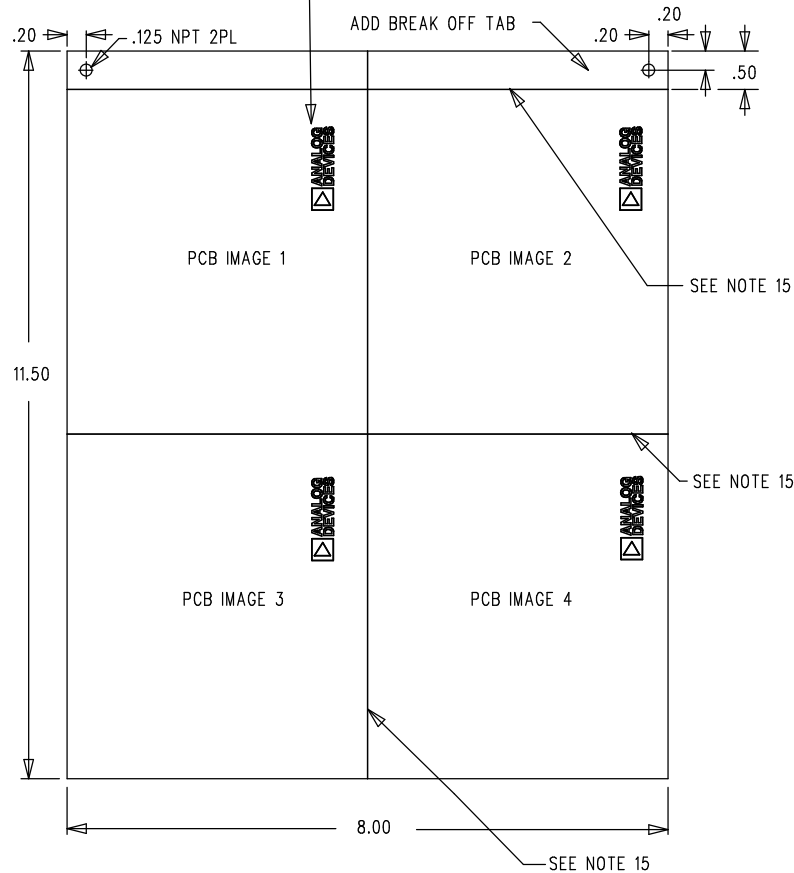


REVISIONS				
REV	DESCRIPTION OF CHANGE	DRFTR	DATE	APPROVED
1.0	NEW RELEASE	EASTERN CIRCUITS	09/26/05	

PANEL DETAIL

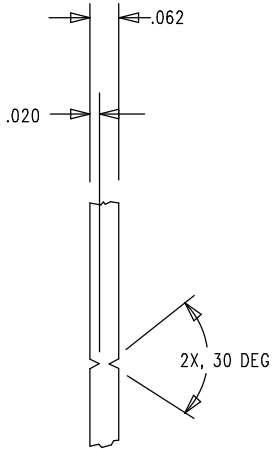
REFERENCE FOR BOARD ORIENTATION



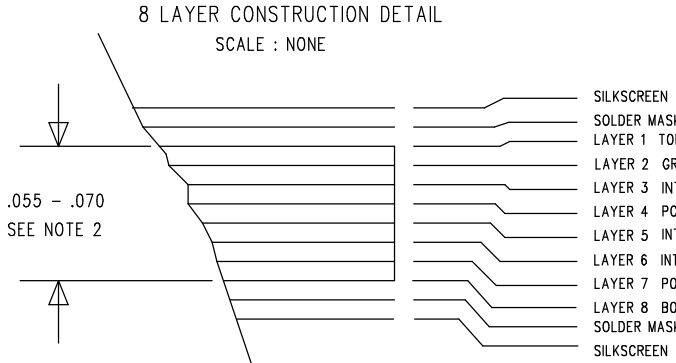
UNLESS OTHERWISE SPECIFIED


- BOARD TO BE FABRICATED PER IPC-6012A, CLASS 2.
- MATERIAL: POLYCLAD FR-370HR OR EQUIVALENT. OUTER LAYERS 1/2 OZ/SQFT CU INNER LAYERS 1/2 OZ/SQFT CU FINISHED .062 (.055 MIN. .070 MAX SEE DETAIL). VENDOR MAY ADJUST THICKNESS TO FULFILL NOTE 9.
- PLATING: ADDITIONAL CU PLATING 1 OZ/SQFT ALL HOLES PLATED THROUGH, EXCEPT AS NOTED IN HOLE LEGEND. MINIMUM PTH BARREL THICKNESS = 0.0008" MINIMUM AVERAGE PER IPC-6012A WITH AMENDMENT 1, CLASS 2 REQUIREMENTS. WITH NO SINGLE MEASUREMENT LESS THAN 0.00071 IN THE PLATED HOLES.
- FINISH: SURFACES TO BE COATED BY ENIG OF 2 TO 10 MICROINCHES OVER A MINIMUM OF 60-200 MICROINCHES OF LOW STRESS NICKEL.
- SOLDERMASK: SOLDER MASK TO BE TRANSPARENT GREEN LPI BOTH SIDES PER GERBER FILES.
- SILKSCREEN: WHITE EPOXY INK, APPLY TO TOP SIDE PER GERBER FILE.
- ARTWORK: MINIMUM FEATURE SIZE = 0.00394 MINIMUM AIR GAP = 0.00394
- ALL DIMENSIONS ARE IN INCHES.
- CONTROLLED IMPEDANCE: BOARD TO BE BUILT TO YIELD CONTROLLED IMPEDANCE OF 50 OHMS - 70 OHMS ON ALL .00394" LINE WIDTHS
- DO NOT ADD NON-FUNCTIONAL COPPER THIEVING ON OPEN AREAS OF OUTER LAYERS.
- VIAS SHOULD BE COVERED ACCORDING TO ONE OF THE FOLLOWING METHODS. METHOD 1 IS PREFERRED.
METHOD 1: VIAS MUST BE FILLED WITH SOLDERMASK MATERIAL AFTER ELECTROLESS NICKEL/IMMERSION GOLD AND BEFORE PRIMARY LPI MASK. AFTER THE FILL IS CURED, THE PRIMARY MASK IS THEN APPLIED WITH NO VIA APERTURES BOTH SIDES.
METHOD 2: AFTER APPLICATION OF FULL BODY ELECTROLESS NICKEL/IMMERSION GOLD, APPLY PRIMARY MASK WITH REDUCED VIA APERTURES THAT ARE 6 MILS LARGER THAN DRILLED HOLE DIAMETER BOTH SIDES. THEN APPLY SOLDER MASK PLUG ON COMPONENT SIDE.
- VIA HOLES (.010) REQUIRE TANGENCY ONLY, INSTEAD OF ANNULAR RING.
- TEARDROP PADS ARE ACCEPTABLE WHERE NEEDED.
- USE IPC-D-356A NETLIST AS SUPPLIED FOR CHECKING.
- V SCORE 3 LINES ON BOTH SIDES OF THE PANEL. SEE DETAIL.
- SEE PANEL DETAIL FOR PANALIZATION.
- WHEN STEP AND REPEAT IS COMPLETE A SOLDERPASTE MASK (GERBER FILE) IS NEED FOR THE ASSEMBLY HOUSE FOR THE PANEL.
PLEASE SUPPLY TO CHIRAG PATEL AT ANALOG DEVICES.

HOLE SIZE CHART			
SYMBOL	DIAMETER	QTY	PLATE
+	.010 +.003/- .010	1371	YES
x	.028 +/- .003	122	YES
□	.037 +/- .003	397	YES
◇	.041 +.003/- .000	22	YES
⊗	.125 +/- .005	3	YES
⊠	.053 +.003/- .000	6	NO



SCORING DETAIL



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE : .XX +/- .010 .XXX +/- .005		CONTRACT NO.		 <div>20 Cotton Road Nashua, New Hampshire 03063 (603) 883-2430 FAX (603) 882-2655</div>		
		APPROVALS	DATE			
MATERIAL	SEE NOTES	DRAWN EASTERN CIRCUITS	09/26/05	FABRICATION DRAWING BLACKFIN FPGA EZ-EXTENDER		
		CHECKED				
FINISH	SEE NOTES	ENGINEERING		SIZE B DWG. NO. A0199-2005 REV. 1.0		
		QUALITY				
DO NOT SCALE THIS DRAWING		MANUFACTURING		SCALE 1 : 1		SHEET 1 OF 1