ADP1046 Evaluation Software

Preliminary Technical Data

EVAL-ADP1046-GUI-RG

GENERAL DESCRIPTION

This user guide describes the various controls and indicators of the ADP1046 Evaluation Software. It gives the details of what each button on the GUI does in terms of the register that is being updated, along with a brief description.

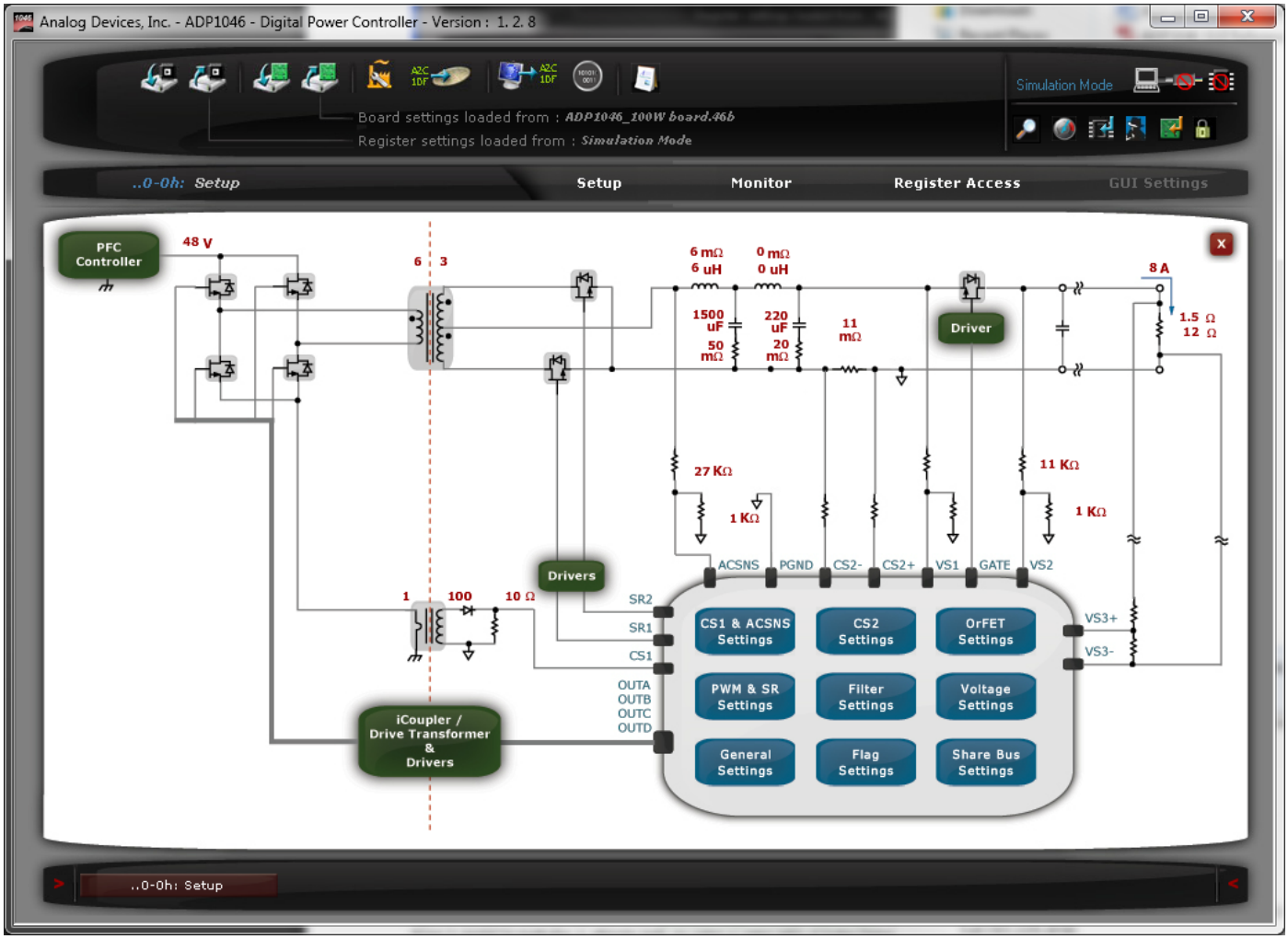

Figure 1. GUI Main Interface Window

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

GUI CONTROLS

LINK

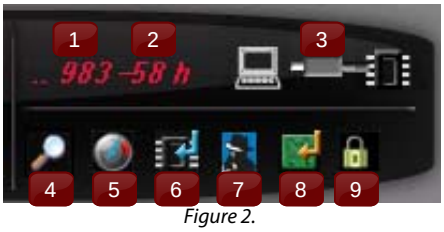

Figure 2.

Table 1. Referring to Figure 2.

No.	Name	REG	Bits	R/W	Description
1	"USB to I2C interface" Number				This number shows the last three digits of the "USB to I2C interface" connected to ADP1046. This number is also physically printed on the "USB to I2C Interface".
2	ADP ADP1046 Address				This number shows the address of ADP1046 the GUI is connected to.
3	Communication link				This animated indicator shows if the GUI is communicating with ADP1046.
4	Scan				The GUI scans for all the ADP1046 connected to the computer. This helps in connecting and disconnecting devices once the GUI is already running.
5	Save/Load Options				This control opens the Tools window.
6	Dashboard				This control opens the Dashboard window.
7	Spy				This control opens the Spy window.
8	Update EEPROM	0x88	[7:0]	W	This control writes the contents of the registers to the EEPROM of ADP1046.
9	Lock / Unlock	0x89	[7:0]	R/W	This control locks or unlocks write-access for Trim registers.

STRUCTURAL NAVIGATION

Figure 3.

Table 2. Referring to Figure 3.

No.	Name	REG	Bits	R/W	Description
1	Device – Window Info				This indicator shows the device address and the window name of the window which is currently open.
2	Structural Navigation				If you have only one device connected to the GUI, then clicking on the buttons opens the respective windows. If you have multiple devices connected, then clicking on the buttons opens the window for the device selected in the "Link" section shown above in Figure 2.

WINDOWS NAVIGATION

Figure 4.

Table 3. Referring to Figure 4.

No.	Name	REG	Bits	R/W	Description
1	Arrows				The arrows move the tabs in the respective directions.
2	Tabs				The tabs open the window whose name and device address is displayed on it.

TOOLS

Figure 5.

Table 4. Referring to Figure 5.

No.	Name	REG	Bits	R/W	Description
1	Save Register Settings				This control saves the contents of the register map of the device selected in the "Link" section shown above in Figure 2, to either a ".46r" file.
2	Load register Settings				This control loads the contents of the register map to the device selected in the "Link" section shown above in Figure 2, from either a ".46r" file.
3	Save Board Settings				This control saves the information about the extrenal components required by the GUI to either a ".46r" file.
4	Load Board Settings				This control loads the information about the extrenal components required by the GUI from either a ".46r" file.
5	Load Factory Trim Values				
6	EEPROM Access				
7	Generates Hex File				This control saves the contents of the register map of the device selected in the "Link" section shown above in Figure 2, to either a ".hex" file.
8	Checksum				This control opens the window, which lets you compare the settings in the part and the settings in a previously saved ".46r" file
9	Reference Guide				This control opens the GUI Reference Guide.

DASHBOARD

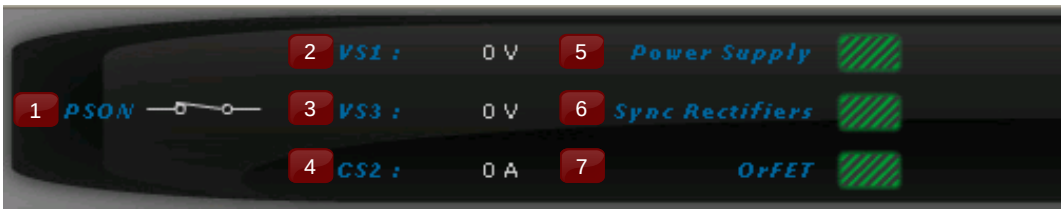

Figure 6.

Table 5. Referring to Figure 6.

No.	Name	REG	Bits	R/W	Description
1	PS ON	0x2C	[5]	R/W	This switch sets the power supply on or off.
2	VS1	0x15	[15:4]	R	This indicator displays the local output voltage measured at the VS1 pin.
3	VS3	0x17	[15:4]	R	This indicator displays the remote output voltage information. This value is the differential voltage between the VS3+ and VS3- pins.
4	CS2	0x18	[15:4]	R	This indicator displays the output current information. This information is the voltage drop across the sense resistor.
5	Power Supply	0x00	[7]	R	Red = Power supply is off. All PWM outputs are disabled. This bit stays high until the power supply is restarted.
6	Sync Rectifiers	0x00	[3]	R	Red = Synchronous rectifiers SR1 and SR2 are disabled. This flag is set when one of the following cases is true: SR1 and SR2 are disabled by the user. The load current has fallen below the threshold in Register 0x3B. A flag has been set that was configured to disable the sync rects.
7	OrFET	0x00	[6]	R/W	Red = The fast OrFET control is disabled.

SETUP

MAIN

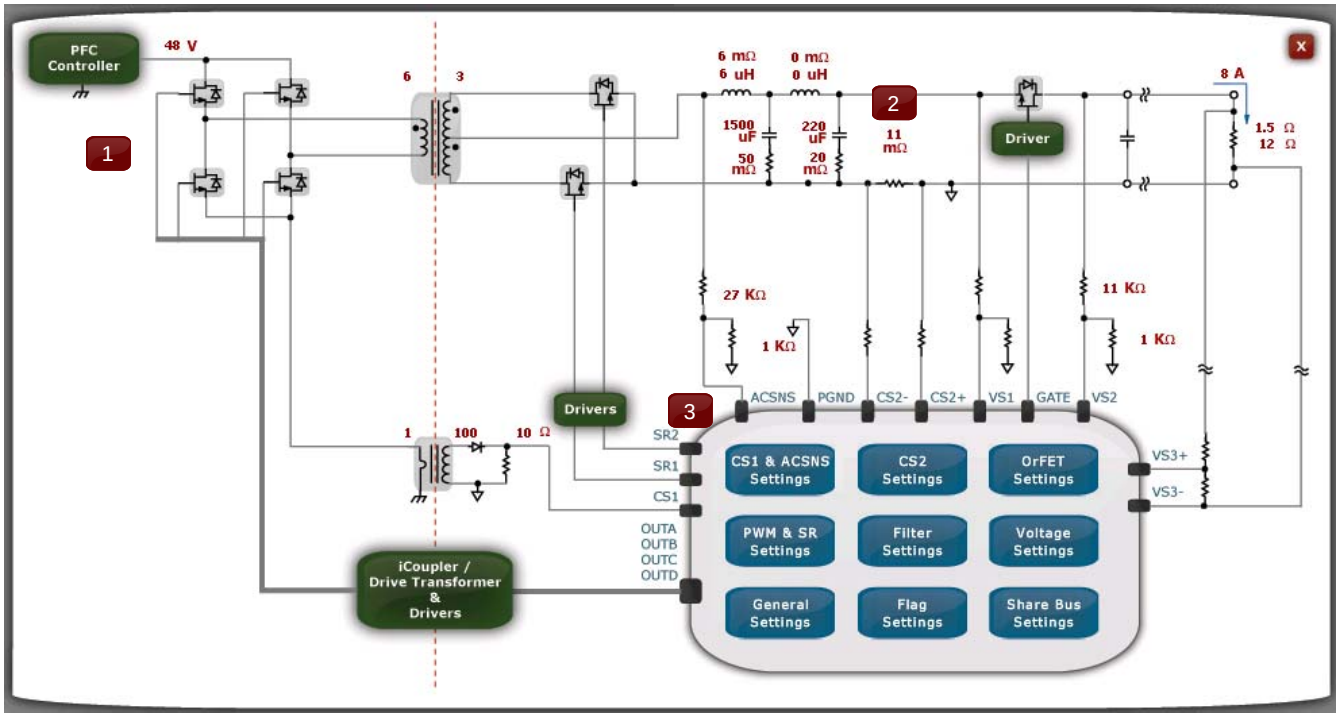

Figure 7.

Table 6. Referring to Figure 7.

No.	Name	REG	Bits	R/W	Description
1	Select Topology	0x40	[5:0]	R/W	If a topology is changed, the switching frequency of all the PWM pins are changed to the corresponding value.
2	Sense Location	0x27	[2]	R/W	This sets either high-side current sensing or low-side current sensing.
3	ADP1046 Setup Blocks				The grey block represents ADP1046 and the blue blocks represent the various setup blocks of the ADP1046. These blue blocks can be clicked to open the corresponding windows for settings.

CS1 & ACSNS SETTINGS

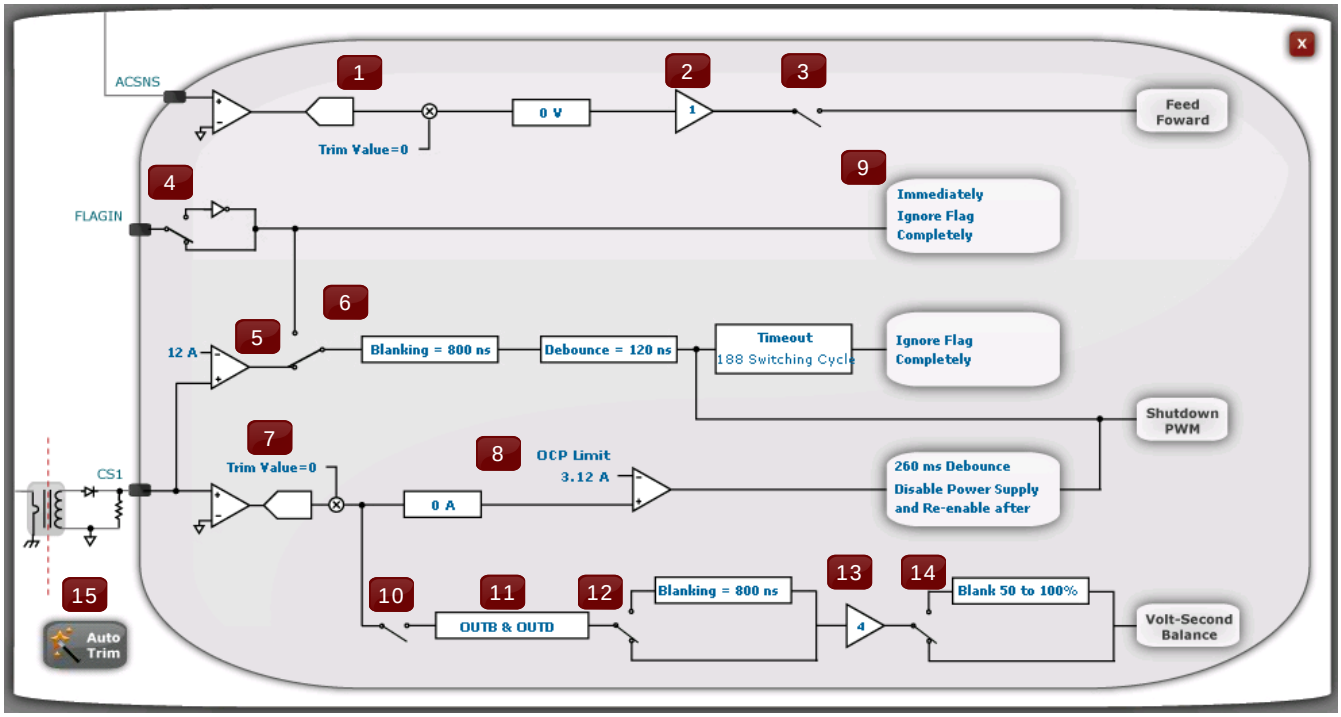

Figure 8.

Table 7. Referring to Figure 8.

No.	Name	REG	Bits	R/W	Description
1	ACSNS Gain Trim Value	0x5E	[7:0]	R/W	This sets the gain trim for the ACSNS ACC.
2	Gain Settings	0x75	[1:0]	R/W	This sets the gain for the voltage feed forward.
3	Feed Forward Enable	0x75	[2:2]	R/W	By closing this switch, it enables voltage feed forward loop.
		0x7F	[3]	R/W	This latches all the filter registers: 0x5F to 0x67 and 0x71 to 0x75.
4	FLAGIN Polarity	0x2D	[2]	R/W	This sets the polarity of the FLAGIN input.
5	CS1 Fast OCP Bypass	0x27	[4]	R/W	This can connect the FLAGIN to either CS1 fast OCP or the CS1 pin.
6	CS1 Fast OCP Blanking	0x22	[7:5]	R/W	This sets the blanking time for CS1 before fast OCP is enabled.
	CS1 Fast OCP Debounce	0x27	[7:6]	R/W	This sets the CS1 fast OCP debounce value.
	CS1 Fast OCP Timeout	0x27	[1:0]	R/W	This sets the number of consecutive switching cycles for the comparator before the CS1 fast OCP flag is set.
7	CS1 Trim Value	0x21	[7:0]	R/W	This sets the primary side current sense gain.

Table 8. Referring to Figure 8.

No.	Name	REG	Bits	R/W	Description
8	CS1 OCP Limit	0x22	[4:0]	R/W	This sets the CS1 accurate OCP threshold.
9	FLAGIN	0x0A	[3]	R/W	This specifies when the flag is set.
			[2:0]	R/W	This specifies the action that the part takes in response to the flag.
	CS1 Fast OCP	0x08	[7]	R/W	This specifies when the flag is set.
			[6:4]	R/W	This specifies the action that the part takes in response to the flag.
	CS1 Accurate OCP	0x0E	[4:2]	R/W	This sets the debounce time of CS1 Accurate OCP.
		0x08	[3]	R/W	This specifies when the flag is set.
			[2:0]	R/W	This specifies the action that the part takes in response to the flag.
10	VS Balance Enable	0x28	[6]	R/W	By closing this switch, it enables volt-second balance for the main transformer.
11	Edges to Measure Current for VSB	0x42	[0]	R/W	This sets OUTA rising edge as start of integration period for Volt-Second balance.
		0x46	[0]	R/W	This sets OUTB rising edge as start of integration period for Volt-Second balance.
		0x4A	[0]	R/W	This sets OUTC rising edge as start of integration period for Volt-Second balance.
		0x4E	[0]	R/W	This sets OUTD rising edge as start of integration period for Volt-Second balance.
12	VS Balance Leading Edge Blanking	0x28	[5]	R/W	This switch makes CS1 blanked for volt-sec balance calculations at the rising edge of those PWM selected for VS balance.
13	VS Balance Gain Setting	0x28	[1:0]	R/W	This sets gain of the volt-second balance circuit.
14	50% Blanking of Each Phase	0x28	[3]	R/W	This switch limits the sampling period for the current on CS1 to less than 50% of half cycle.
15	Auto Trim	0x21	[7:0]	R/W	This can be clicked for automatic trim.
		0x42	[0]	R/W	
		0x46	[0]	R/W	
		0x4A	[0]	R/W	
		0x4E	[0]	R/W	

CS2 SETTINGS

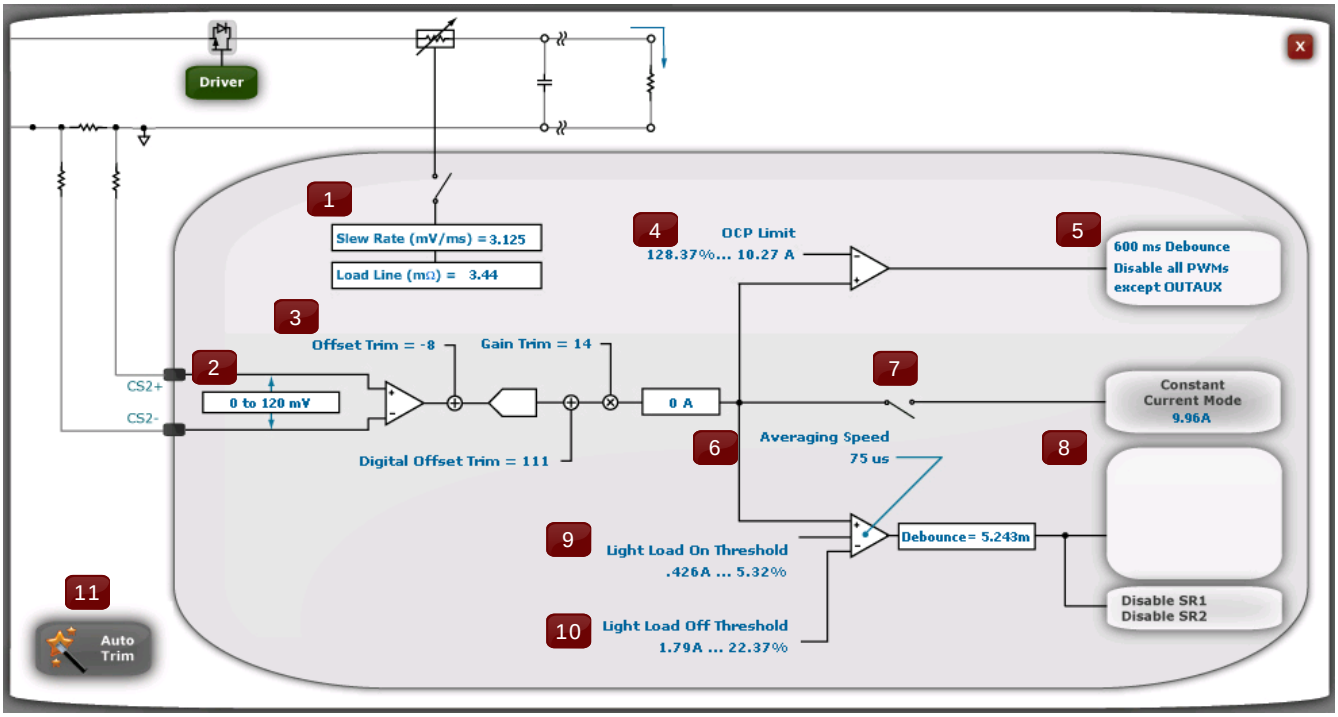

Figure 9.

Table 9. Referring to Figure 9.

No.	Name	REG	Bits	R/W	Description
1	Slew Rate	0x36	[6:4]	R/W	This sets the max slew rate for changing the reference when adjusting output load line value.
	Load Line		[2:0]	R/W	This sets how much the output voltage decreases from nominal at full load.
2	Range	0x27	[5]	R/W	This sets the nominal full-scale voltage drop across the sense resistor.
3	CS2 Offset Trim	0x24	[6:0]	R/W	This sets the secondary side (CS2) current sense common-mode error.
	CS2 Gain Trim	0x23	[5:0]	R/W	This sets the secondary side (CS2) current sense gain.
	CS2 Digital Offset Trim	0x25	[7:0]	R/W	This sets the CS2 digital trim level.
4	CS2 OCP Limit	0x26	[7:0]	R/W	This sets the CS2 accurate OCP current level.
5	CS2 Accurate OCP	0x0E	[4:2]	R/W	This sets the delay for CS2 Accurate OCP.
		0x09	[7]	R/W	This specifies when the flag is set.
			[6:4]	R/W	This specifies the action that the part takes in response to the flag.

Table 10. Referring to Figure 9.

No.	Name	REG	Bits	R/W	Description
6	Averaging Speed	0x7D	[3:2]	R/W	This sets the averaging speed and resolution used for the light load thresholds.
7	Constant Current Mode	0x27	[3]	R/W	By closing this switch, it enables constant current mode.
8	Light Load Mode Disable Setting	0x3B	[7:3]	R/W	These enable or disable OUTA, OUTB, OUTC, OUTD and OUTAUX.
9	Light Load On Threshold	0x3B	[2:0]	R/W	This sets the load current limit on the CS2 ADC below which the synchronous rectifier outputs (SR1 and SR2) are diabled.
	Debounce	0x7D	[5:4]	R/W	This sets the debounce time.
10	Light Load Off Threshold	0x7D	[1:0]	R/W	This sets the amount of hysteresis applied to the light load mode thresholds.
11	Auto Trim	0x38 0x39	[7:0] [7:0]	R/W R/W	This can automatically trim VS1 and VS2.

ORFET SETTINGS

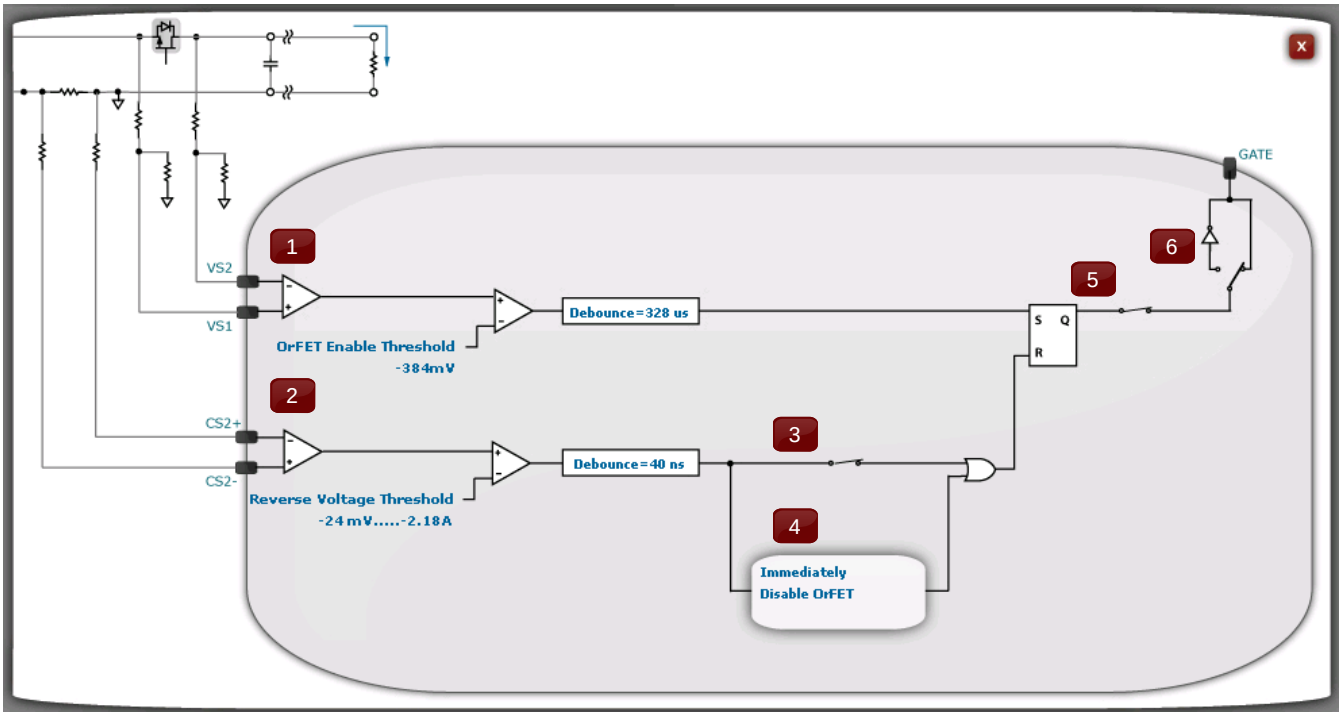

Figure 10.

Table 11. Referring to Figure 10.

No.	Name	REG	Bits	R/W	Description
1	OrFET Enable Threshold	0x30	[6:5]	R/W	This sets the voltage difference between VS1 and VS2 before the OrFET is enabled.
	OrFET Enable Speed	0x30	[7]	R/W	This sets the speed of OrFET.
2	Fast OrFET Threshold	0x30	[4:2]	R/W	This sets the threshold voltage difference between CS2+ and CS2- at which the OrFET is disabled.
	Fast OrFET Debounce	0x30	[1]	R/W	This sets the debounce on the fast OrFET control before it disables the OrFET.
3	Fast OrFET Bypass	0x30	[0]	R/W	By closing this switch, it bypasses the fast OrFET control.
4	CS2 Reverse Voltage timing	0x0C	[7]	R/W	This sets when the flag is set.
	CS2 Reverse Voltage Action	0x0C	[6:4]	R/W	This sets the action that part takes in response to the flag.
5	GATE Disable	0x5D	[0]	R/W	By closing this switch, it disables the GATE output.
6	GATE Polarity	0x2D	[1]	R/W	By closing this switch, it changes the polarity of the OrFET GATE control pin.

PWM & SR SETTINGS – MAIN (GENERAL)

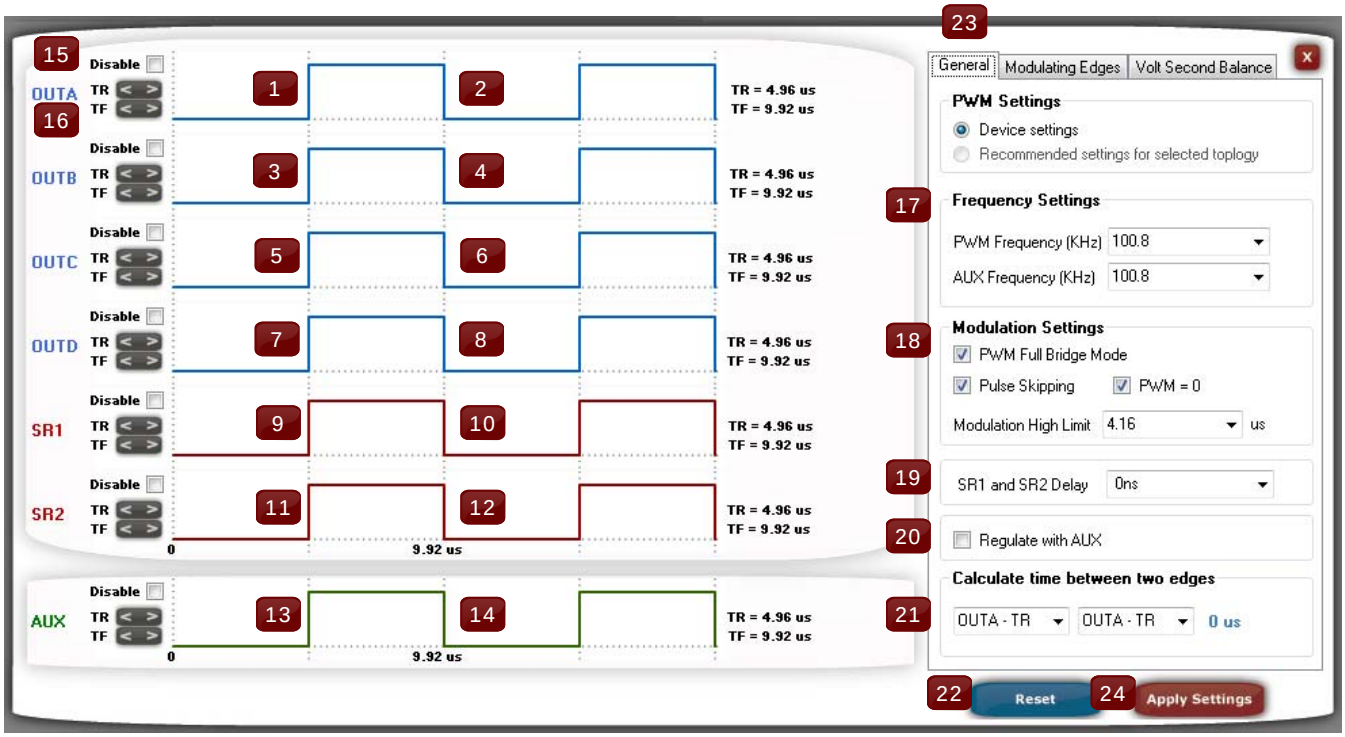

Figure 11.

Table 12. Referring to Figure 11.

No.	Name	REG	Bits	R/W	Description
1	OUTA Rising Edge Timing	0x41 0x42	[7:0] [7:4]	R/W R/W	This sets OUTA Rising Edge timing.
2	OUTA Falling Edge Timing	0x43 0x44	[7:0] [7:4]	R/W R/W	This sets OUTA Falling Edge timing.
3	OUTB Rising Edge Timing	0x45 0x46	[7:0] [7:4]	R/W R/W	This sets OUTB Rising Edge timing.
4	OUTB Falling Edge Timing	0x47 0x48	[7:0] [7:4]	R/W R/W	This sets OUTB Falling Edge timing.
5	OUTC Rising Edge Timing	0x49 0x4A	[7:0] [7:4]	R/W R/W	This sets OUTC Rising Edge timing.
6	OUTC Falling Edge Timing	0x4B 0x4C	[7:0] [7:4]	R/W R/W	This sets OUTC Falling Edge timing.
7	OUTD Rising Edge Timing	0x4D 0x4E	[7:0] [7:4]	R/W R/W	This sets OUTD Rising Edge timing.
8	OUTD Falling Edge Timing	0x4F 0x50	[7:0] [7:4]	R/W R/W	This sets OUTD Falling Edge timing.

Table 13. Referring to Figure 11.

No.	Name	REG	Bits	R/W	Description
9	SR1 Rising Edge Timing	0x51 0x52	[7:0] [7:4]	R/W R/W	This sets SR1 Rising Edge timing.
10	SR1 Falling Edge Timing	0x53 0x54	[7:0] [7:4]	R/W R/W	This sets SR1 Falling Edge timing.
11	SR2 Rising Edge Timing	0x55 0x56	[7:0] [7:4]	R/W R/W	This sets SR2 Rising Edge timing.
12	SR2 Falling Edge Timing	0x57 0x58	[7:0] [7:4]	R/W R/W	This sets SR2 Falling Edge timing.
13	OUTA UX Rising Edge Timing	0x59 0x5A	[7:0] [7:4]	R/W R/W	This sets OUTA UX Rising Edge timing.
14	OUTA UX Falling Edge Timing	0x5B 0x5C	[7:0] [7:4]	R/W R/W	This sets OUTA UX Falling Edge timing.
15	OUTx and SRx Pin Disable Setting	0x5D	[7:1]	R/W	These disable the corresponding PWM output.
16	OUTx, SRx and AUX TR TF	0x42 0x44 0x46 0x48 0x4A 0x4C 0x4E 0x50 0x52 0x54 0x56 0x58 0x5A 0x5C	[2] [2] [2] [2] [2] [2] [2] [2] [2] [2] [2] [2] [2] [2]	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W	This moves rising edge or falling edge left or right.
17	**Frequency Settings** PWM Frequency AUX Frequency	0x40 0x3F	[5:0] [5:0]	R/W R/W	This sets the switching frequency of all the PWM pins other than the OUTAUX pin. This sets the switching frequency of the OUTAUX signal.
18	**Modulation Settings** PWM Full Bridge Mode Pulse Skipping PWM = 0 Modulation High Limit	0x2E 0x3F 0x3F 0x2E	[7] [7] [6] [6:0]	R/W R/W R/W R/W	This enables Full-bridge mode. This enables Pulse Skipping mode. This sets all modulated edges to t=0. This sets the min/max modulation limits relative to the nominal edge value.

Table 14. Referring to Figure 11.

No.	Name	REG	Bits	R/W	Description
19	SR1 and SR2 Delay	0x79	[5:0]	R/W	This sets the SR delay in steps of 5ns.
20	Regulate with AUX	0x5C	[1]	R/W	This can be checked to regulate control loop PWM modulation by OUTAUX.
21	Calculate time between two edges				It calculates the time difference between two edges.
22	Reset				This button loads the settings programmed in the ADP1046 connected to the software.
23	Tabs				These tabs can be clicked to open setting windows.
24	Apply Settings				This control programs all the PWM settings to the part.

PWM & SR SETTINGS – MAIN (MODULATING EDGES)

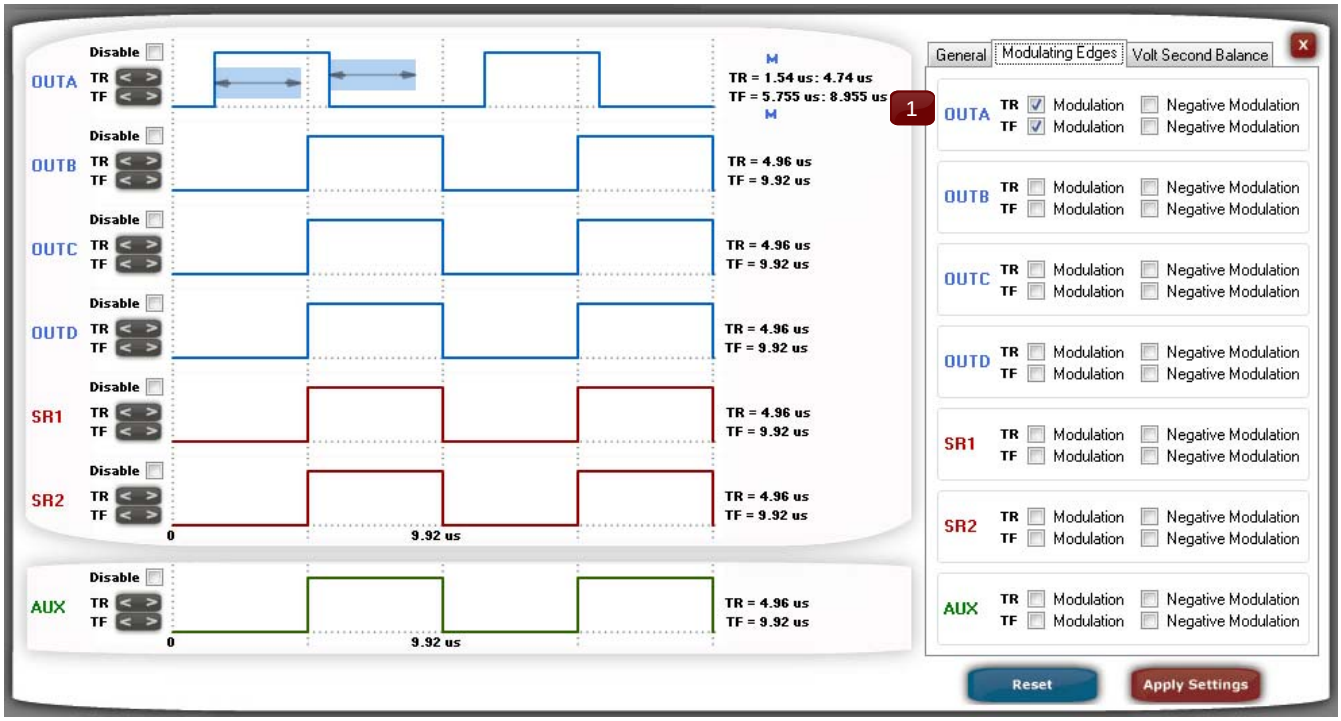

Figure 12.

Table 15. Referring to Figure 12.

No.	Name	REG	Bits	R/W	Description
1	OUTx, SRx and AUX Modulation Enable	0x42	[3]	R/W	This enables PWM modulation acting on the corresponding edge.
		0x44	[3]	R/W	
		0x46	[3]	R/W	
		0x48	[3]	R/W	
		0x4A	[3]	R/W	
		0x4C	[3]	R/W	
		0x4E	[3]	R/W	
		0x50	[3]	R/W	
		0x52	[3]	R/W	
		0x54	[3]	R/W	
		0x56	[3]	R/W	
		0x58	[3]	R/W	
		0x5A	[3]	R/W	
		0x5C	[3]	R/W	

PWM & SR SETTINGS – MAIN (VOLT SECOND BALANCE)

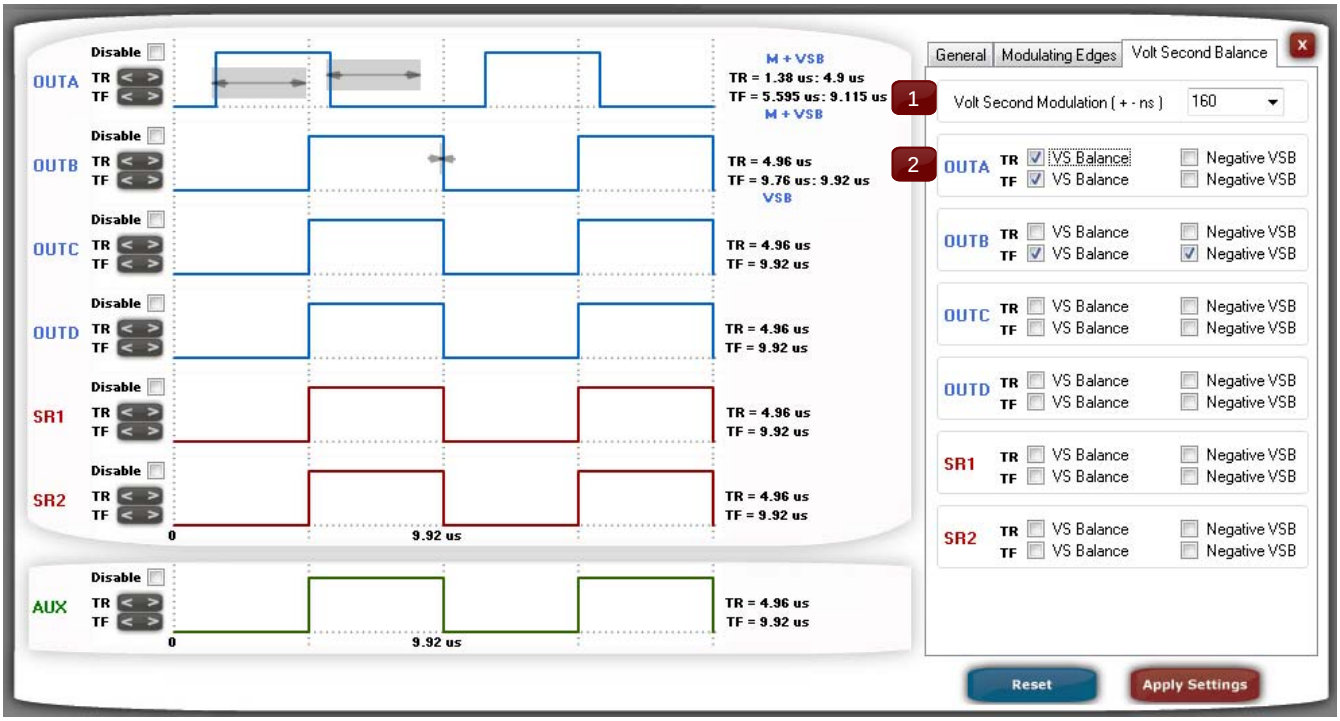

Figure 13.

Table 16. Referring to Figure 13.

No.	Name	REG	Bits	R/W	Description
1	Volt Second Balance Modulation	0x28	[2]	R/W	This sets the max amount of modulation from Volt Second Balance.
2	OUTx, SRx and AUX VS Balance	0x42 0x44 0x46 0x48 0x4A 0x4C 0x4E 0x50 0x52 0x54 0x56 0x58 0x5A 0x5C	[0] [0] [0] [0] [0] [0] [0] [0] [0] [0] [0] [0] [0] [0]	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W	This enables the corresponding edge as start of integration period for Volt Second Balance.

Table 17. Referring to Error! Reference source not found.

No.	Name	REG	Bits	R/W	Description
10	SR1 R Dead Time	0x6D	[7:4]	R/W	This sets the dead time for SR1 R.
11	SR1 F Dead Time	0x6D	[3:0]	R/W	This sets the dead time for SR1 F.
12	SR2 R Dead Time	0x6E	[7:4]	R/W	This sets the dead time for SR2 R.
13	SR2 F Dead Time	0x6E	[7:4]	R/W	This sets the dead time for SR2 F.
14	AUX R Dead Time	0x6F	[3:0]	R/W	This sets the dead time for AUX R.
15	AUX F Dead Time	0x6F	[7:4]	R/W	This sets the dead time for AUX F.
16	Max Range	0x70	[2:0]	R/W	This sets the max range of the Dead Time.
17	PWM window				This shows the PWM window.
18	The difference between Edge1 and Edge2				It calculates the time difference between two edges.
19	Dead Time Update Rate	0x70	[5:3]	R/W	This sets the number of PWM switching cycles between each step.
20	Averaging Time	0x70	[7:6]	R/W	This sets the averaging period for CS1 used to set the adaptive dead time.
21	Apply Settings				This control programs all the above values to the corresponding registers and bits.

FILTER SETTINGS

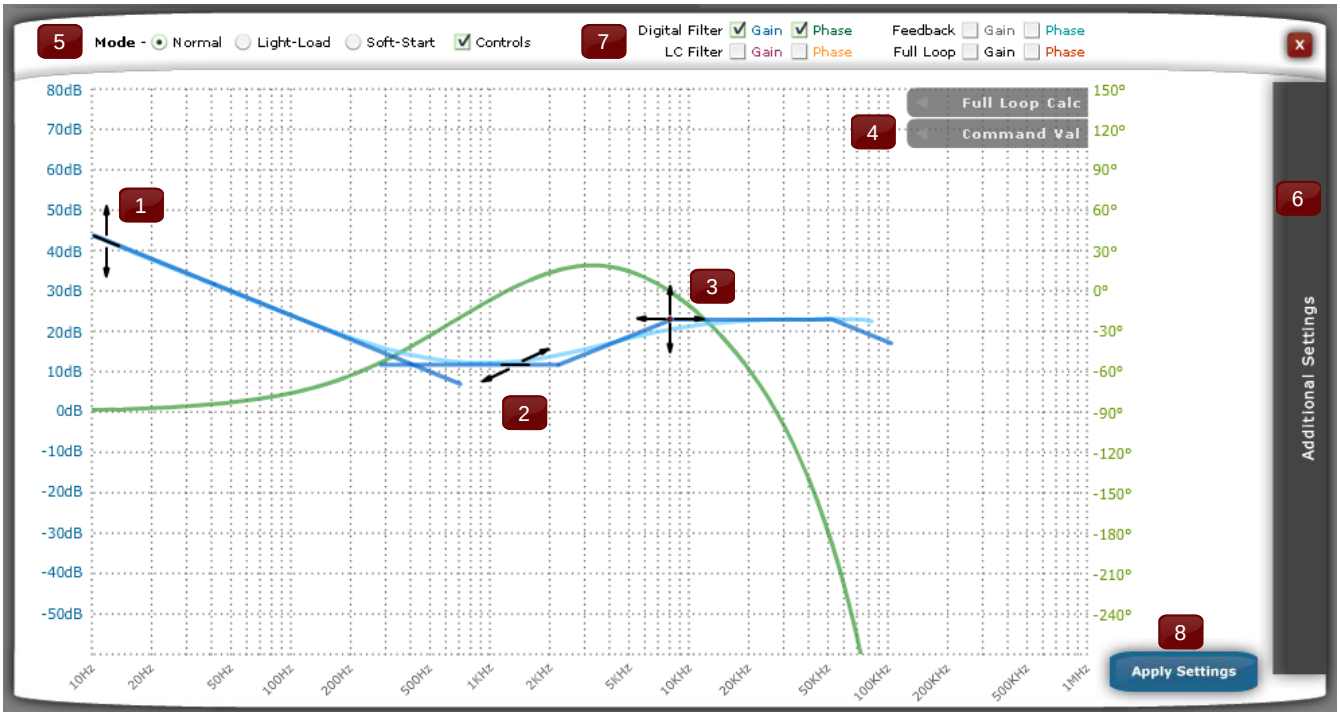

Figure 14.

Table 18. Referring to Figure 14.

No.	Name	REG	Bits	R/W	Description
1	Up-Down Arrows				This arrow can be moved top and down which sets the Low Frequency Gain for the corresponding filter selected
2	Side Ways Arrows				This arrow can be moved top and down at 20db/decade slope, which sets the location of the zero for the corresponding filter selected
3	Four Way Arrows				This arrow can be moved top and down and left-right, the top-down action sets the HF Gain and the left-right action sets the location of the pole for the corresponding filter selected
4	Display Reg Values				This shows LF Gain, Zero, Pole and HF Gain values as the corresponding graph changes.
5	Mode				This sets the mode of filter settings.
6	Copy Filter Settings to				A filter setting can be copied to the other modes through this button.
7	Enable Plot				If the checkbox is enabled, then the corresponding graph will be plotted.
8	Apply Settings				This control programs all the above values to the corresponding registers and bits.

VOLTAGE SETTINGS

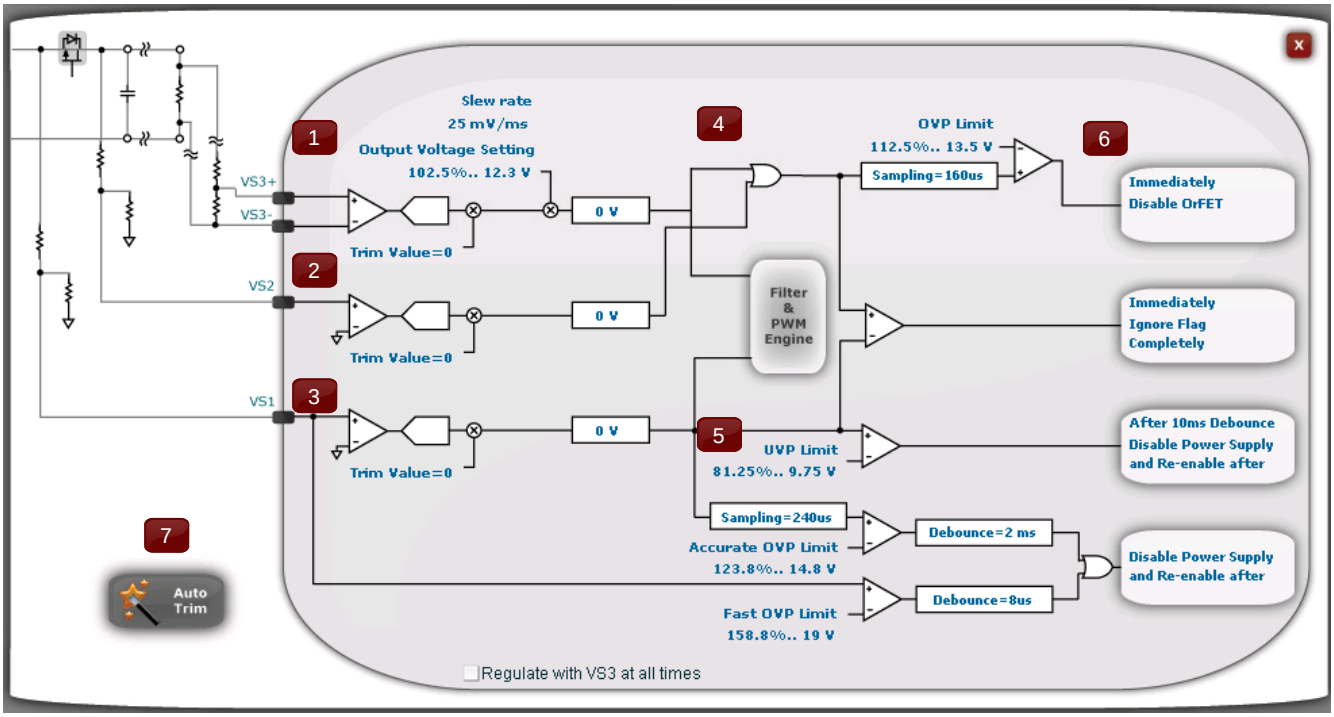

Figure 15.

Table 19. Referring to Figure 15.

No.	Name	REG	Bits	R/W	Description
1	Slew Rate	0x5F	[2:0]	R/W	The voltage reference setting change slew rate.
	Output Voltage Setting	0x7F 0x31	[0] [7:0]	R/W R/W	This sets the output voltage (Voltage difference at the VS3+ and VS3- pins).
	VS3 Trim Value	0x3A	[7:0]	R/W	This sets the amount of gain trim that is applied to the VS3 ADC reading.
2	VS2 Trim Value	0x39	[7:0]	R/W	This sets the amount of trim that is applied to the VS2 ADC reading.
3	VS1 Trim Value	0x38	[7:0]	R/W	This sets the amount of trim that is applied to the VS1 ADC reading.
4	VS3 OVP Limit	0x33	[7:3]	R/W	This sets the local overvoltage limit.
	VS3 Sampling	0x33	[1:0]	R/W	This sets the VS3 Sampling period.

Table 20. Referring to Figure 15.

No.	Name	REG	Bits	R/W	Description
5	VS1 UVP Limit	0x34	[6:0]	R/W	This sets the UVP limit to one of 128 settings.
	VS1 Sampling	0x32	[1:0]	R/W	This sets the VS1 Sampling period.
	VS1 Accurate OVP Limit	0x32	[7:3]	R/W	This sets the local overvoltage limit.
	VS1 Accurate OVP Debounce	0x0A	[7:4]	R/W	This sets the Accurate OVP debounce time.
	VS1 Fast OVP Limit	0x37	[5:0]	R/W	This sets the threshold for the Fast OVP analog comparator.
	VS1 Fast OVP Debounce	0x37	[7:6]	R/W	This sets the Fast OVP debounce time.
6	Load OVP (VS2 / VS3) Timing	0x09	[3]	R/W	This specifies when the flag is set.
	Load OVP (VS2 / VS3) Action	0x09	[2:0]	R/W	This specifies the action that the part takes in response to the flag.
	Voltage Continuity Timing	0x0C	[3]	R/W	This specifies when the flag is set.
	Voltage Continuity Action	0x0C	[2:0]	R/W	This specifies the action that the part takes in response to the flag.
	Local UVP Timing	0x0B	[3]	R/W	This specifies when the flag is set.
	Local UVP Action	0x0B	[2:0]	R/W	This specifies the action that the part takes in response to the flag.
	Local OVP Action	0x0A	[7:4]	R/W	This specifies the action that the part takes in response to the flag.
7	Auto Trim	0x38 0x39	[7:0] [7:0]	R/W R/W	This can automatically trim VS1 and VS2.

GENERAL SETTINGS - MAIN

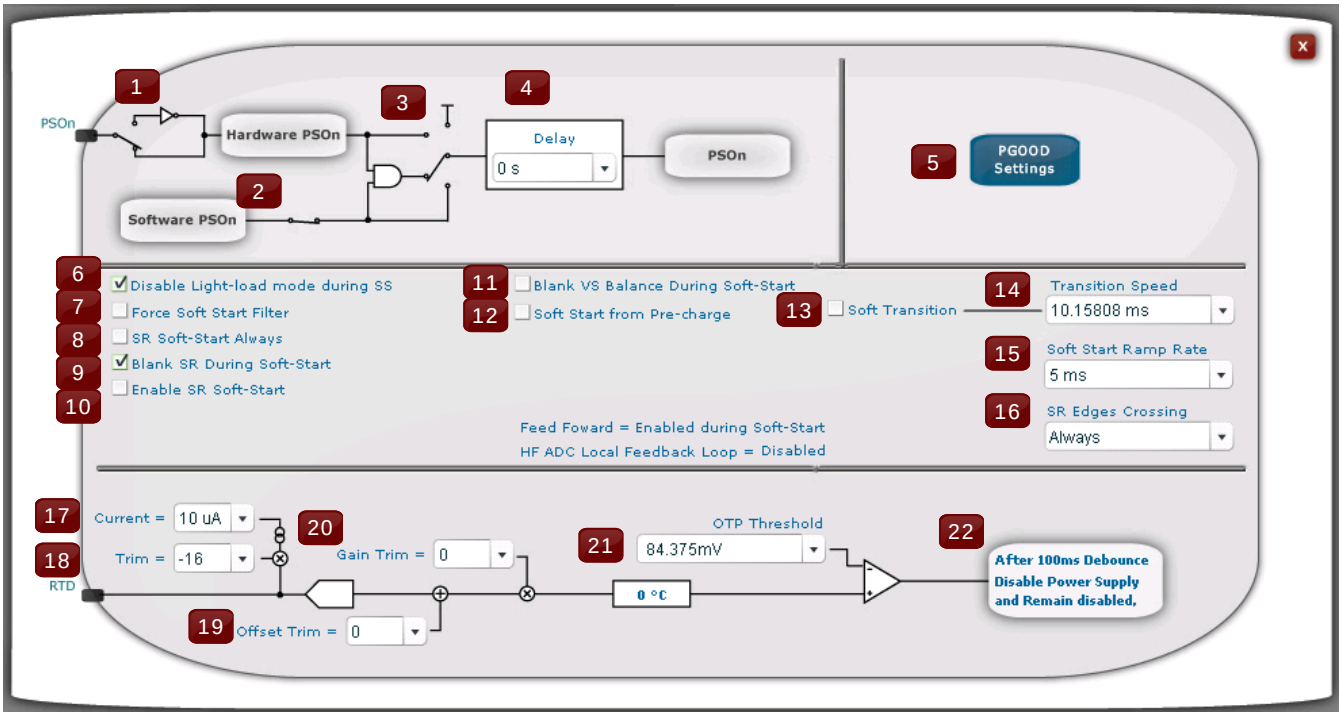

Figure 16.

Table 21. Referring to Figure 16.

No.	Name	REG	Bits	R/W	Description
1	PSOn Polarity	0x2D	[0]	R/W	This sets the polarity of the PSOn input pin.
2	PSOn	0x2C	[5]	R/W	This sets Software PSOn on and off.
3	PSOn Setting	0x2C	[7:6]	R/W	This sets which signal is used by the ADP1046 as the PSOn control.
4	PSOn Delay	0x2C	[4:3]	R/W	This sets the time from when the PSOn control signal is set to when the Soft Start begins.
5	PGOOD Settings				This opens PGOOD Settings window.
6	Disable Light-load mode during SS	0x2C	[1]	R/W	This enables or disables Light-load mode during Soft Start.
7	Force Soft Start filter	0x2C	[0]	R/W	This forces a part to use SS Filter regardless of OrFET status.
8	SR Soft Start Always	0x54	[1]	R/W	This sets SR signals to perform a soft start every time or only first time.
9	Blank ST During Soft Start	0x0F	[7:0]	R/W	This disables the SR1 and SR2 PWM outputs until the end of the Soft Start ramp time.
10	Enable SR Soft Start	0x54 0x7F	[0] [7:0]	R/W R/W	This enables the Soft Start function for the SR signals.
11	Blank VS Balance During Soft Start	0x28	[4]	R/W	This can be set to blank Volt-second Balance control during Soft Start.
12	Soft Start from Pre-charge	0x5F	[4]	R/W	This enables the Soft Start from per charge function.

Table 22. Referring to Figure 16.

No.	Name	REG	Bits	R/W	Description
13	Soft Transition	0x7A	[2]	R/W	This enables Soft Transition between filter settings to minimize output transients.
14	Transition Speed	0x7A	[1:0]	R/W	This sets the transition speed.
15	Soft Start Ramp Rate	0x5F	[7:5]	R/W	This sets the duration of the Soft Start Ramp.
16	SR Edges Crossing	0x52	[0]	R/W	This can be set to allow SR Edge Crossing always or only during SR-SS.
17	Current	0x11	[7:6]	R/W	This sets the size of the current source on the RTD1 pin.
18	Trim	0x11	[5:0]	R/W	This sets the trim value for the current source on the RTD pin.
19	Offset Trim	0x1C 0x20	[1:0] [7:0]	R/W R/W	This sets the amount of offset trim that is applied to the RTD ADC reading.
20	Gain Trim	0x2B	[7:0]	R/W	This sets the RTD ADC gain.
21	OTP Threshold	0x2F	[7:0]	R/W	This sets OPT Threshold value.
22	OPT	0x0B	[7] [6:4]	R/W R/W	This sets when the flag is set. This sets the action that the part takes in response to the flag.

GENERAL SETTINGS – PGOOD SETTINGS

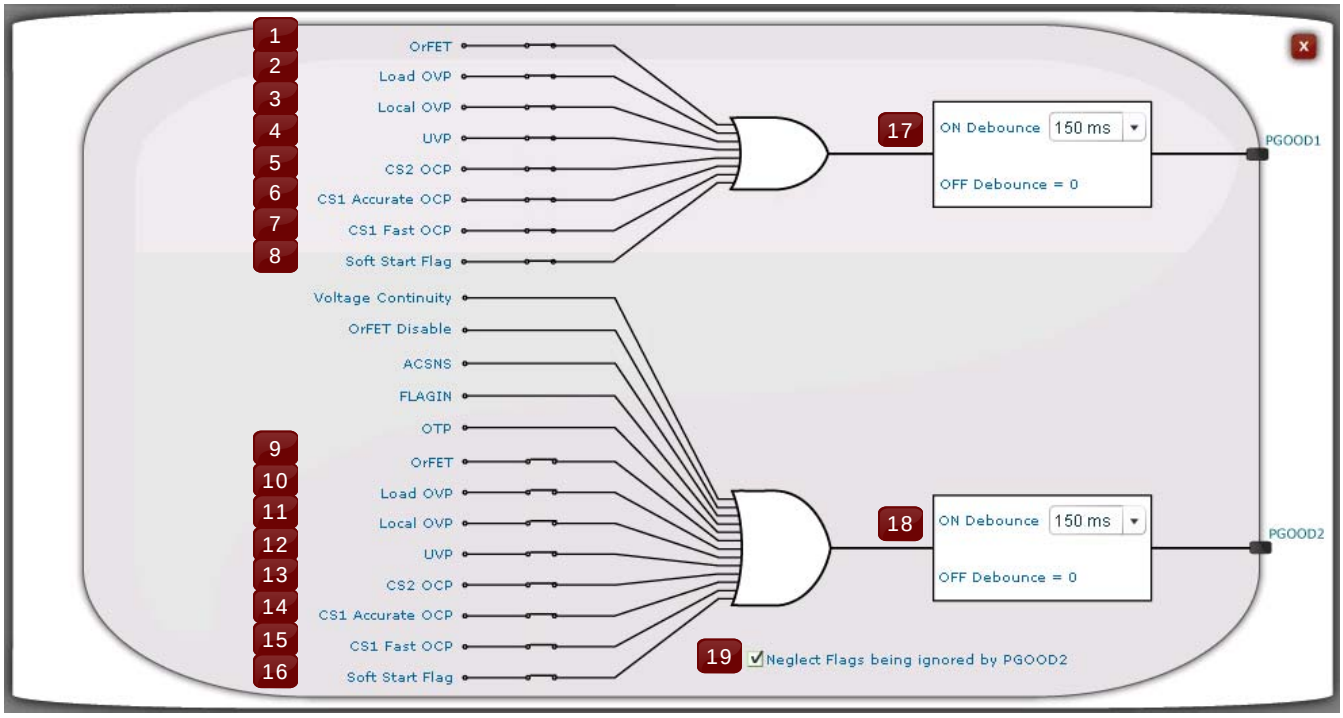

Figure 17.

Table 23. Referring to Figure 17.

No.	Name	REG	Bits	R/W	Description
1	OrFET	0x7B	[0]	R/W	If this switch is opened, this flag will be ignored by PGOOD1.
2	Load OVP	0x7B	[1]	R/W	If this switch is opened, this flag will be ignored by PGOOD1.
3	Local OVP	0x7B	[2]	R/W	If this switch is opened, this flag will be ignored by PGOOD1.
4	UVP	0x7B	[3]	R/W	If this switch is opened, this flag will be ignored by PGOOD1.
5	CS2 OCP	0x7B	[4]	R/W	If this switch is opened, this flag will be ignored by PGOOD1.
6	CS1 Accurate OCP	0x7B	[5]	R/W	If this switch is opened, this flag will be ignored by PGOOD1.
7	CS1 Fast OCP	0x7B	[6]	R/W	If this switch is opened, this flag will be ignored by PGOOD1.
8	Soft Start Flag	0x7B	[7]	R/W	If this switch is opened, this flag will be ignored by PGOOD1.
9	OrFET	0x7B	[0]	R/W	If this switch is opened, this flag will be ignored by PGOOD2.
10	Load OVP	0x7B	[1]	R/W	If this switch is opened, this flag will be ignored by PGOOD2.
11	Local OVP	0x7B	[2]	R/W	If this switch is opened, this flag will be ignored by PGOOD2.

Table 24. Referring to Figure 17.

No.	Name	REG	Bits	R/W	Description
12	UVP	0x7B	[3]	R/W	If this switch is opened, this flag will be ignored by PGOOD2.
13	CS2 OCP	0x7B	[4]	R/W	If this switch is opened, this flag will be ignored by PGOOD2.
14	CS1 Accurate OCP	0x7B	[5]	R/W	If this switch is opened, this flag will be ignored by PGOOD2.
15	CS1 Fast OCP	0x7B	[6]	R/W	If this switch is opened, this flag will be ignored by PGOOD2.
16	Soft Start Flag	0x7B	[7]	R/W	If this switch is opened, this flag will be ignored by PGOOD2.
17	On Debounce PGOOD1	0x2D	[7:6]	R/W	This sets the debounce time before the PGOOD1 pin and the flag is set.
18	On Debounce PGOOD2	0x2D	[5:4]	R/W	This sets the debounce time before the PGOOD2 pin and the flag is set.
19	Neglect Flags being ignored by PGOOD2	0x2D	[3]	R/W	If this is checked, any flag that has not been configured to be ignored can set the PGOOD2 pin.

FLAG SETTINGS

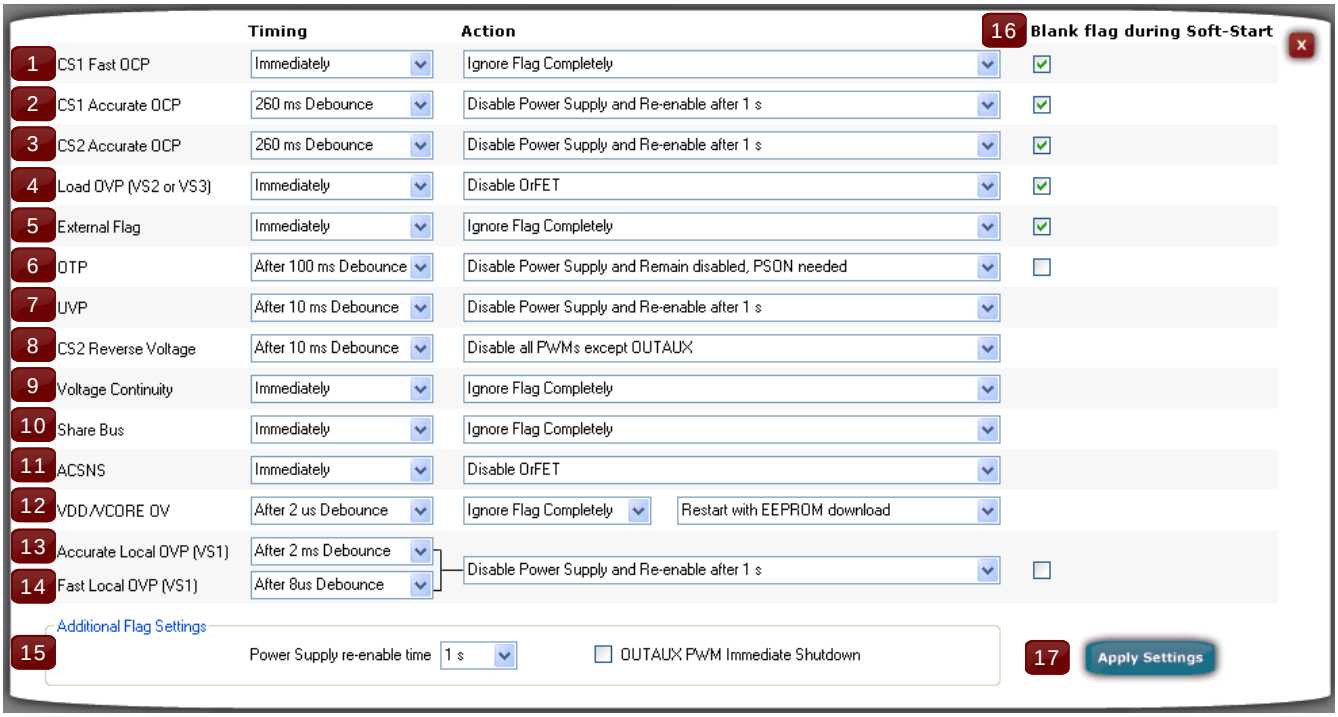

Figure 18.

Table 25. Referring to Figure 18.

No.	Name	REG	Bits	R/W	Description
1	CS1 Fast OCP Timing	0x08	[7]	R/W	This sets when the flag is set.
	CS1 Fast OCP Action	0x08	[6:4]	R/W	This sets the action that the part takes in response to the flag.
2	CS1 Accurate OCP Timing	0x0E 0x08	[4:2] [3]	R/W	This sets the debounce before te corresponding action is performed. This sets when the flag is set.
	CS1 Accurate OCP Action	0x08	[2:0]	R/W	This sets the action that the part takes in response to the flag.
3	CS2 Accurate OCP Timing	0x0E 0x09	[4:2] [7]	R/W	This sets the debounce before te corresponding action is performed. This sets when the flag is set.
	CS2 Accurate OCP Action	0x09	[6:4]	R/W	This sets the action that the part takes in response to the flag.
4	Load OVP (VS2 or VS3) Timing	0x09	[3]	R/W	This sets when the flag is set.
5	Load OVP (VS2 or VS3) Action	0x09	[2:0]	R/W	This sets the action that the part takes in response to the flag.
	External Flag Timing	0x0A	[3]	R/W	This sets when the flag is set.
	External Flag Action	0x0A	[2:0]	R/W	This sets the action that the part takes in response to the flag.
6	OTP Timing	0x0B	[7]	R/W	This sets when the flag is set.
	OTP Action	0x0B	[6:4]	R/W	This sets the action that the part takes in response to the flag.
7	UVP Timing UVP Action	0x0B 0x0B	[3] [2:0]	R/W R/W	This sets when the flag is set. This sets the action that the part takes in response to the flag.

Table 26. Referring to Figure 18.

No.	Name	REG	Bits	R/W	Description
8	CS2 Reverse Voltage Timing	0x0C	[7]	R/W	This sets when the flag is set.
	CS2 Reverse Voltage Action	0x0C	[6:4]	R/W	This sets the action that the part takes in response to the flag.
9	Voltage Continuity OCP Timing	0x0C	[3]	R/W	This sets when the flag is set.
	Voltage Continuity Action	0x0C	[2:0]	R/W	This sets the action that the part takes in response to the flag.
10	Share Bus Timing	0x0D	[7]	R/W	This sets when the flag is set.
	Share Bus Action	0x0D	[3:0]	R/W	This sets the action that the part takes in response to the flag.
11	ACSNS Timing	0x0D	[3]	R/W	This sets when the flag is set.
	ACSNS Action	0x0D	[2:0]	R/W	This sets the action that the part takes in response to the flag.
12	VDD/VCORE OV Timing	0x0E	[5]	R/W	This sets the debounce time before the part shuts down.
	VDD/VCORE OV Flags Ignore	0x0E	[7]	R/W	This can be set to ignore the VDD OC and VCORE OV flags.
	VDD/VCORE OV Flags Restart	0x0E	[6]	R/W	This can be set to download the EEPROM contents again before restarting.
13	Accurate Local OVP (VS1) Timing	0x0A	[7]	R/W	This sets when the flag is set.
	Accurate Local OVP (VS1) Action	0x0A	[6:4]	R/W	This sets the action that the part takes in response to the flag.
14	Fast Local OVP Timing	0x37	[7:6]	R/W	This sets the Fast OVP debounce time.
	Fast Local OVP Action	0x0A	[6:4]	R/W	This sets the action that the part takes in response to the flag.
15	Power Supply re-enable Time	0x0E	[1:0]	R/W	This sets the time delay before restarting the power supply after a shutdown.
	OUTAUX PWM Immediate Shutdown	0x34	[7]	R/W	This can be set to shut down all other PWM outputs immediately.
16	Blank flag during Soft-Start	0x0F	[7:0]	R/W	These can be set to ignore the corresponding flag until the end of the soft start ramp time.
17	Apply Settings				This control programs all the above values to the corresponding registers and bits.

SHARE BUS SETTINGS

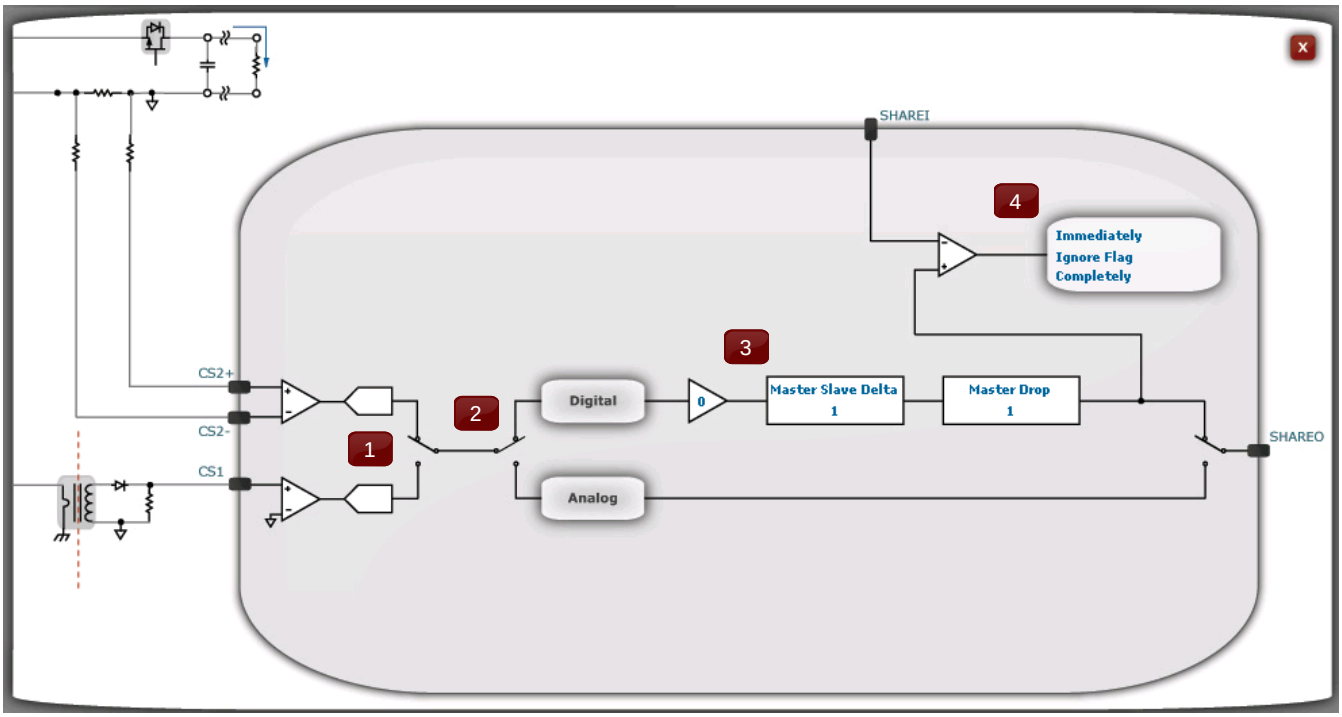

Figure 19.

Table 27. Referring to Figure 19.

No.	Name	REG	Bits	R/W	Description
1	Current Share Select	0x29	[3]	R/W	This can be set to use either CS1 reading or CS2 reading for current share.
2	Bit stream	0x29	[4]	R/W	This can be set to make the current sense ADC reading as output on the SHAREo pin or the digital share bus signal as output on the SHAREo.
3	Gain	0x29	[2:0]	R/W	This sets the amount of bandwidth dedicated to the share bus.
	Difference Between Master and Slave	0x2A	[7:4]	R/W	This sets how closely a slave tries to match the current of the master device.
	Number of LSBs Master is allowed to drop	0x2A	[3:0]	R/W	This sets how much a master device reduces its output voltage to maintain current sharing.
4	Share Bus Timing	0x0D	[7]	R/W	This sets when the flag is set.
	Share Bus Action	0x0D	[6:4]	R/W	This sets the action that the part takes in response to the flag.

MONITOR

MAIN

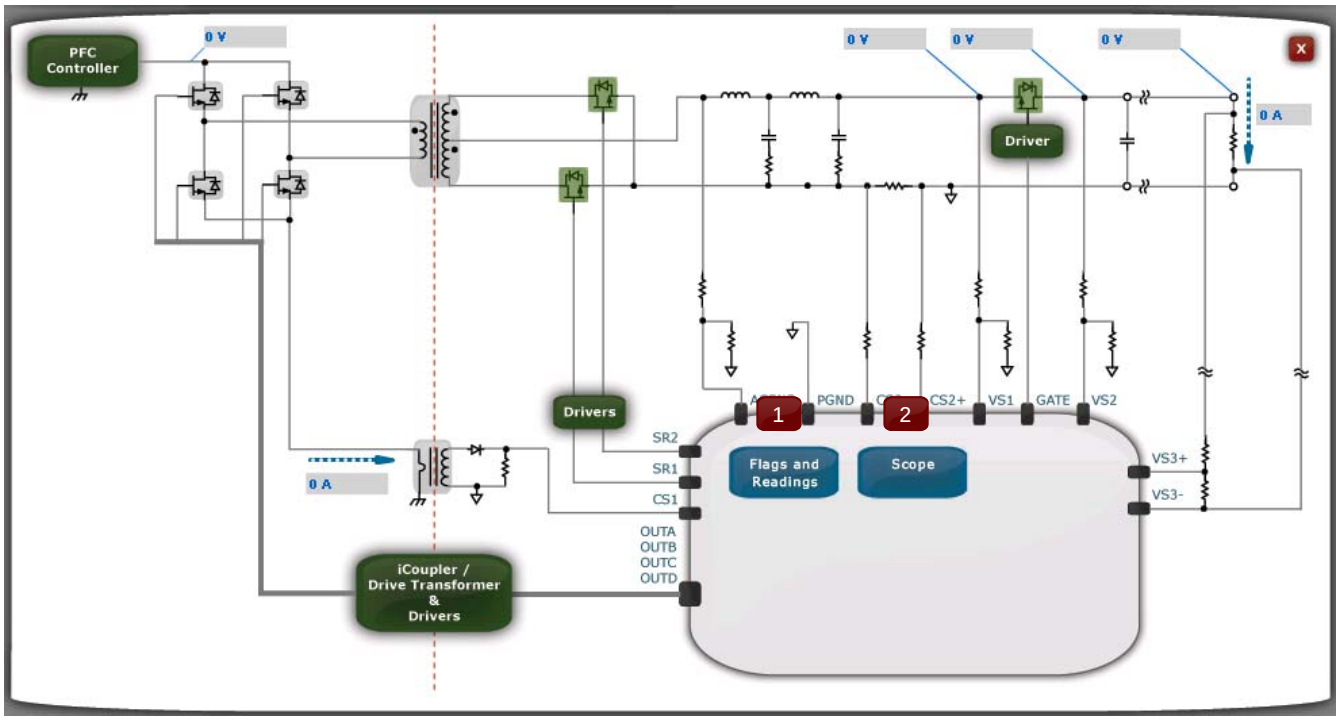

Figure 20.

Table 28. Referring to Figure 20.

No.	Name	REG	Bits	R/W	Description
1	Flag and Readings				The grey block represents ADP1046 and the blue blocks represent the various monitor blocks of them. This blue block can be clicked to open the corresponding window for monitor.
2	Scope				This blue block can be clicked to open the corresponding scope window.

FLAGS AND READINGS

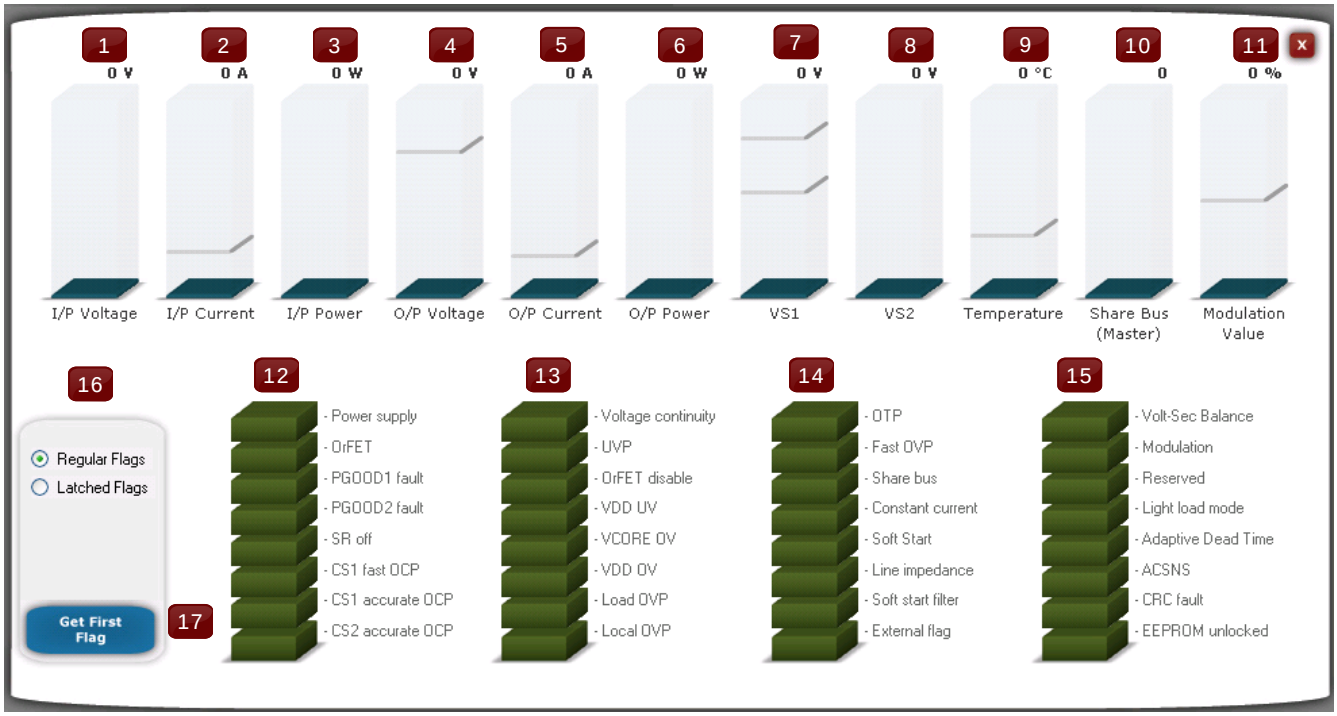

Figure 21.

Table 29. Referring to Figure 21.

No.	Name	REG	Bits	R/W	Description
1	I/P Voltage	0x14	[15:0]	R	This indicator displays the input volt (V).
2	I/P Current	0x13	[15:0]	R	This indicator displays the input current (A).
3	I/P Power		[15:0]	R	This indicator displays the input power (W).
4	O/P Voltage	0x17	[15:0]	R	This indicator displays the remote output volt (V).
5	O/P Current	0x18	[15:0]	R	This indicator displays the output current (A).
6	O/P Power	0x19	[15:0]	R	This indicator displays the output power (W).
7	VS1	0x15	[15:0]	R	This displays the local output voltage information (V).
8	VS2	0x16	[15:0]	R	This displays the load output voltage information (V).
9	Temperature	0x1B	[7:0]	R	This indicator displays the output temperature (°C).
10	Share Bus (Master)	0x1D	[7:0]	R	This indicator displays the share bus voltage.
11	Modulation Value	0x1E	[7:0]	R	This indicator displays the modulation information (%).

Regular Flags - 1

Table 30. Referring to Figure 21.

No.	Name	REG	Bits	R/W	Description
12	Power Supply	0x00	[7]	R	Red = The power supply is off.
	OrFET	0x00	[6]	R	Red = OrFET control signal at the GATE pin (pin 16) is off.
	PGOOD1 fault	0x00	[5]	R	Red = Power-good 1 fault.
	PGOOD2 fault	0x00	[4]	R	Red = Power-good 2 fault.
	SR off	0x00	[3]	R	Red = Synchronous rectifiers SR1 and SR2 are disabled.
	CS1 fast OCP	0x00	[2]	R	Red = CS1 current is above its fast overcurrent protection limit.
	CS1 accurate OCP	0x00	[1]	R	Red = CS1 current is above its accurate overcurrent protection limit.
	CS3 accurate OCP	0x00	[0]	R	Red = CS2 current is above its accurate overcurrent protection limit.
13	Voltage Continuity	0x01	[7]	R	Red = Voltage differential between VS1 and VS2 pins or between VS2 and VS3 pins is outside limits.
	UVP	0x01	[6]	R	Red = VS1 is below its undervoltage limit.
	OrFET disable	0x01	[5]	R	Red = Reverse voltage across VS2 pins is above limit.
	VDD UV	0x01	[4]	R	Red = VDD is below limit.
	VCORE OV	0x01	[3]	R	Red = 2.5V VCORE is above limit.
	VDD OV	0x01	[2]	R	Red = VDD is above limit.
	Load OVP	0x01	[1]	R	Red = VS2 or VS3 is above its overvoltage limit.
	Local OVP	0x01	[0]	R	Red = VS1 is above its overvoltage limit.
14	OTP	0x02	[7]	R	Red = Temperature is above OTP limit.
	Fast OVP	0x02	[6]	R	Red = Fast OVP
	Share bus	0x02	[5]	R	Red = Current share is outside regulation limit.
	Constant current	0x02	[4]	R	Red = Power supply is operating in constant current mode.
	Soft Start	0x02	[3]	R	Red = The reference is being ramped.
	Line impedance	0x02	[2]	R	Red = Line impedance between VS2 and VS3 is above limit.
	Soft Start filter	0x02	[1]	R	Red = The soft start filter is in use.
	External flag	0x02	[0]	R	Red = The external flag pin (FLAGIN) is set.

Regular Flags - 2

Table 31. Referring to Figure 21.

No.	Name	REG	Bits	R/W	Description
15	Volt-Sec Balance	0x03	[7]	R	Red = Volt-second balance is at max/min limit.
	Modulation	0x03	[6]	R	Red = Modulation is at its max/min limit.
	Reserved	0x03	[5]	R	Reserved
	Light load mode	0x03	[4]	R	Red = The system is in light load mode.
	Adaptive Dead Time	0x03	[3]	R	Red = Adaptive Dead Time in use and affecting PWM edges.
	ACSNS	0x03	[2]	R	Red = The AC sense (comparator) amplitude is not correct.
	CRC fault	0x03	[1]	R	Red = The EEPROM contents downloaded are incorrect.
	EEPROM unlocked	0x03	[0]	R	Red = The EEPROM is unlocked.

Latched Flags - 1

Table 32. Referring to Figure 21.

No.	Name	REG	Bits	R/W	Description
12	Power Supply	0x00	[7]	R	Red = The power supply is off.
	OrFET	0x00	[6]	R	Red = OrFET control signal at the GATE pin (pin 16) is off.
	PGOOD1 fault	0x00	[5]	R	Red = Power-good 1 fault.
	PGOOD2 fault	0x00	[4]	R	Red = Power-good 2 fault.
	SR off	0x00	[3]	R	Red = Synchronous rectifiers SR1 and SR2 are disabled.
	CS1 fast OCP	0x00	[2]	R	Red = CS1 current is above its fast overcurrent protection limit.
	CS1 accurate OCP	0x00	[1]	R	Red = CS1 current is above its accurate overcurrent protection limit.
	CS3 accurate OCP	0x00	[0]	R	Red = CS2 current is above its accurate overcurrent protection limit.
13	Voltage Continuity	0x01	[7]	R	Red = Voltage differential between VS1 and VS2 pins or between VS2 and VS3 pins is outside limits.
	UVP	0x01	[6]	R	Red = VS1 is below its undervoltage limit.
	OrFET disable	0x01	[5]	R	Red = Reverse voltage across VS2 pins is above limit.
	VDD UV	0x01	[4]	R	Red = VDD is below limit.
	VCORE OV	0x01	[3]	R	Red = 2.5V VCORE is above limit.
	VDD OV	0x01	[2]	R	Red = VDD is above limit.
	Load OVP	0x01	[1]	R	Red = VS2 or VS3 is above its overvoltage limit.
	Local OVP	0x01	[0]	R	Red = VS1 is above its overvoltage limit.
14	OTP	0x02	[7]	R	Red = Temperature is above OTP limit.
	Fast OVP	0x02	[6]	R	Red = Fast OVP
	Share bus	0x02	[5]	R	Red = Current share is outside regulation limit.
	Constant current	0x02	[4]	R	Red = Power supply is operating in constant current mode.
	Soft Start	0x02	[3]	R	Red = The reference is being ramped.
	Line impedance	0x02	[2]	R	Red = Line impedance between VS2 and VS3 is above limit.
	Soft Start filter	0x02	[1]	R	Red = The soft start filter is in use.
	External flag	0x02	[0]	R	Red = The external flag pin (FLAGIN) is set.

Latched Flags - 2

Table 33. Referring to Figure 21.

No.	Name	REG	Bits	R/W	Description
15	Volt-Sec Balance	0x03	[7]	R	Red = Volt-second balance is at max/min limit.
	Modulation	0x03	[6]	R	Red = Modulation is at its max/min limit.
	Reserved	0x03	[5]	R	Reserved
	Light load mode	0x03	[4]	R	Red = The system is in light load mode.
	Adaptive Dead Time	0x03	[3]	R	Red = Adaptive Dead Time in use and affecting PWM edges.
	ACSNS	0x03	[2]	R	Red = The AC sense (comparator) amplitude is not correct.
	CRC fault	0x03	[1]	R	Red = The EEPROM contents downloaded are incorrect.
	EEPROM unlocked	0x03	[0]	R	Red = The EEPROM is unlocked.
16	**Radio button**	0x00	[7:0]	R	If this button is set, Regular Flags are shown.
	Regular Flags	0x01	[7:0]	R	
		0x02	[7:0]	R	
		0x03	[7:0]	R	
	Latched Flags	0x00	[7:0]	R	If this button is set, Latched Flags are shown.
		0x01	[7:0]	R	
		0x02	[7:0]	R	
		0x03	[7:0]	R	
17	Get First Flag				This can be clicked to get the first flags.

SCOPE

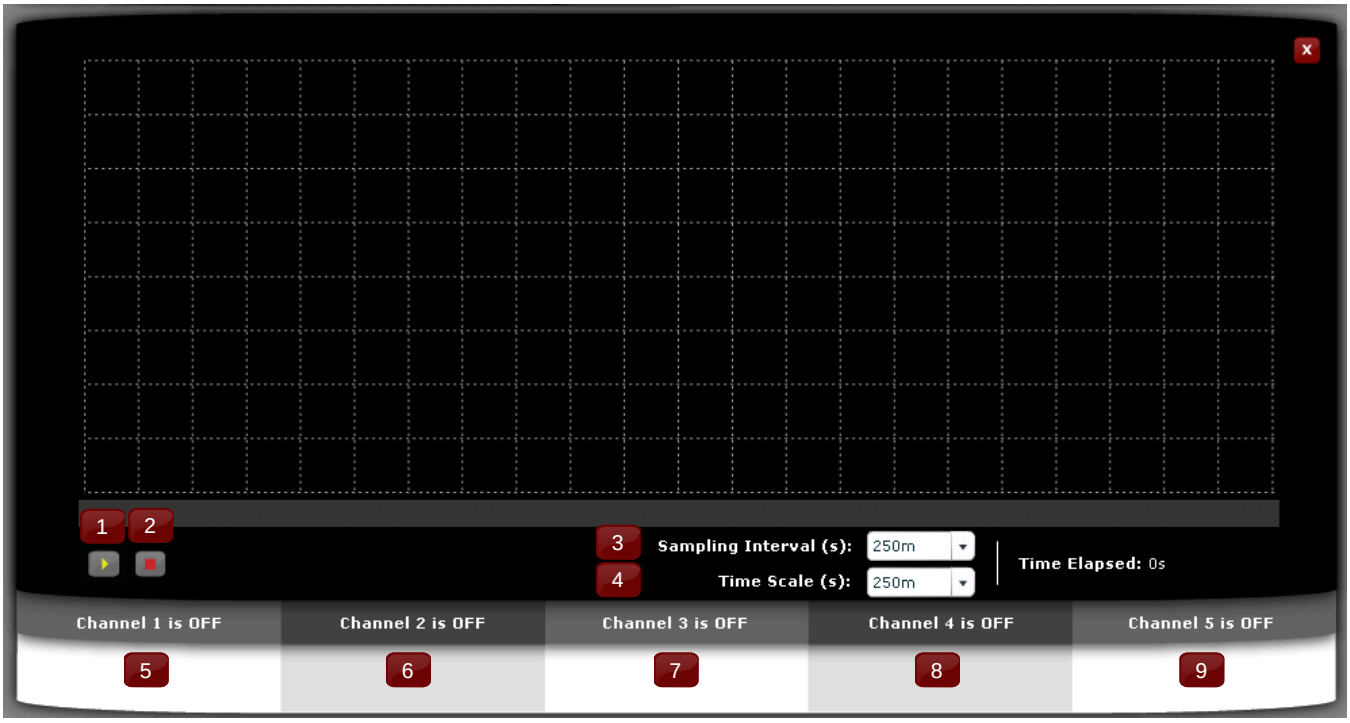

Figure 22.

Table 34. Referring to Figure 22.

No.	Name	REG	Bits	R/W	Description
1	Start button				This can be clicked to start drawing a corresponding graph on the coordinates.
2	Stop button				This can be clicked to stop drawing a graph.
3	Sampling Interval				This sets the sampling interval.
4	Time Scale				This sets the time scale.
5 6 7 8 9	Channel 1 Channel 2 Channel 3 Channel 4 Channel 5				This scope has 5 channels and each of them can measure either one of the 11 readings or one of the 32 flags.

REGISTER ACCESS

MAIN

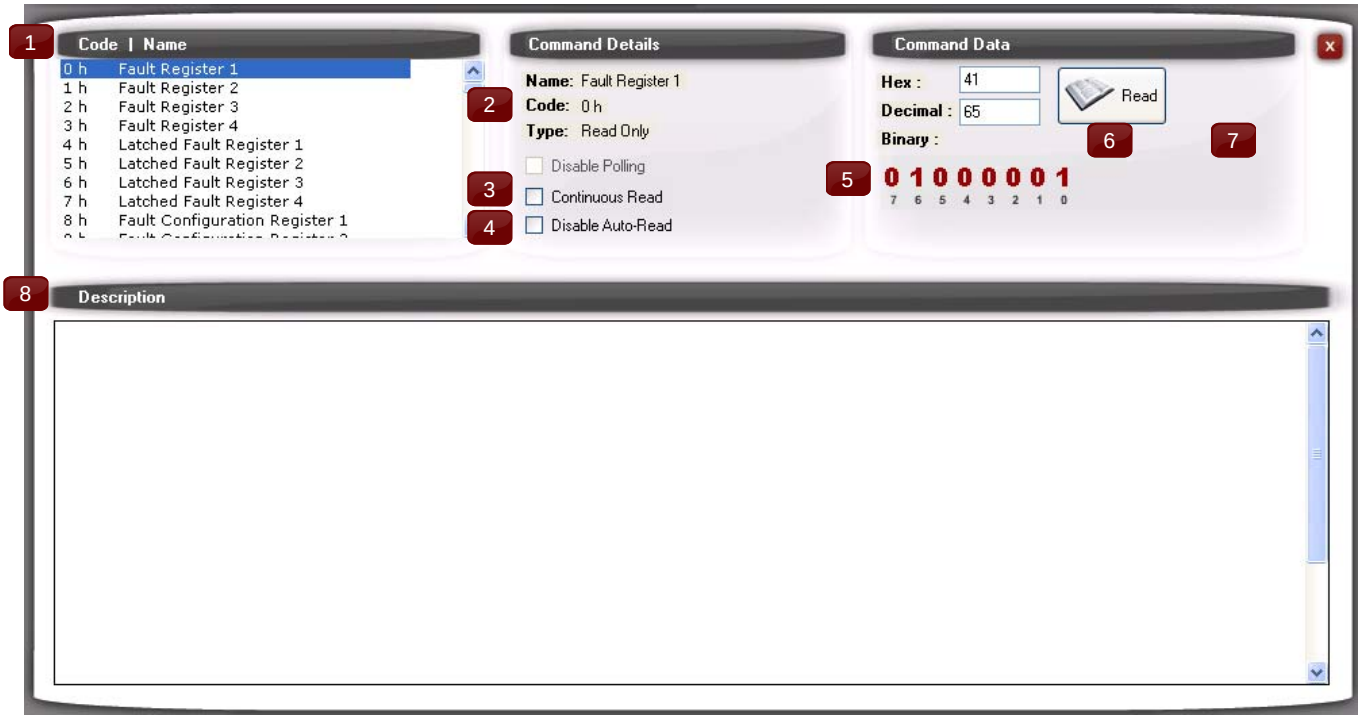

Figure 23.

Table 35. Referring to Figure 23.

No.	Name	REG	Bits	R/W	Description
1	Register Map	0x01 – 0xFE9B			This control displays the complete ADP1046 register map, Selecting any particular register will display the data contained in that register, and will allow this register to be read and written to.
2	Register Details				These set of indicators display the selected register's *(selected in* 1 *)* Command Name, Code and its value in hexadecimal and decimal formats.
3	Continuous Read				If this checkbox is enabled then the GUI will continuously read the value of the register selected in control 1 .
4	Disable Automatic Read-Back				The GUI automatically does a read operation after a write operation to verify if the write operation was successful. Enabling this checkbox disables this automatic read-back feature.
5	Bit Display				This control / indicator displays the current value of the selected register, and can be modified by clicking on the individual bits.
6	Read				This control reads the value of the register selected by control 1.
7	Write				This control writes the value to the register selected by control 1.
8	Description				This indicator displays the description of the selected register.