EVAL-ADP1047/ADP1048-GUI-RG

ADP1047/ADP1048 Evaluation Software Reference Guide

GENERAL DESCRIPTION

The EVAL-ADP1047/ADP1048-GUI-RG user guide describes the various controls and indicators of the ADP1047/ADP1048 evaluation software. It details the functionality of the GUI button for the register being updated along with a brief description.

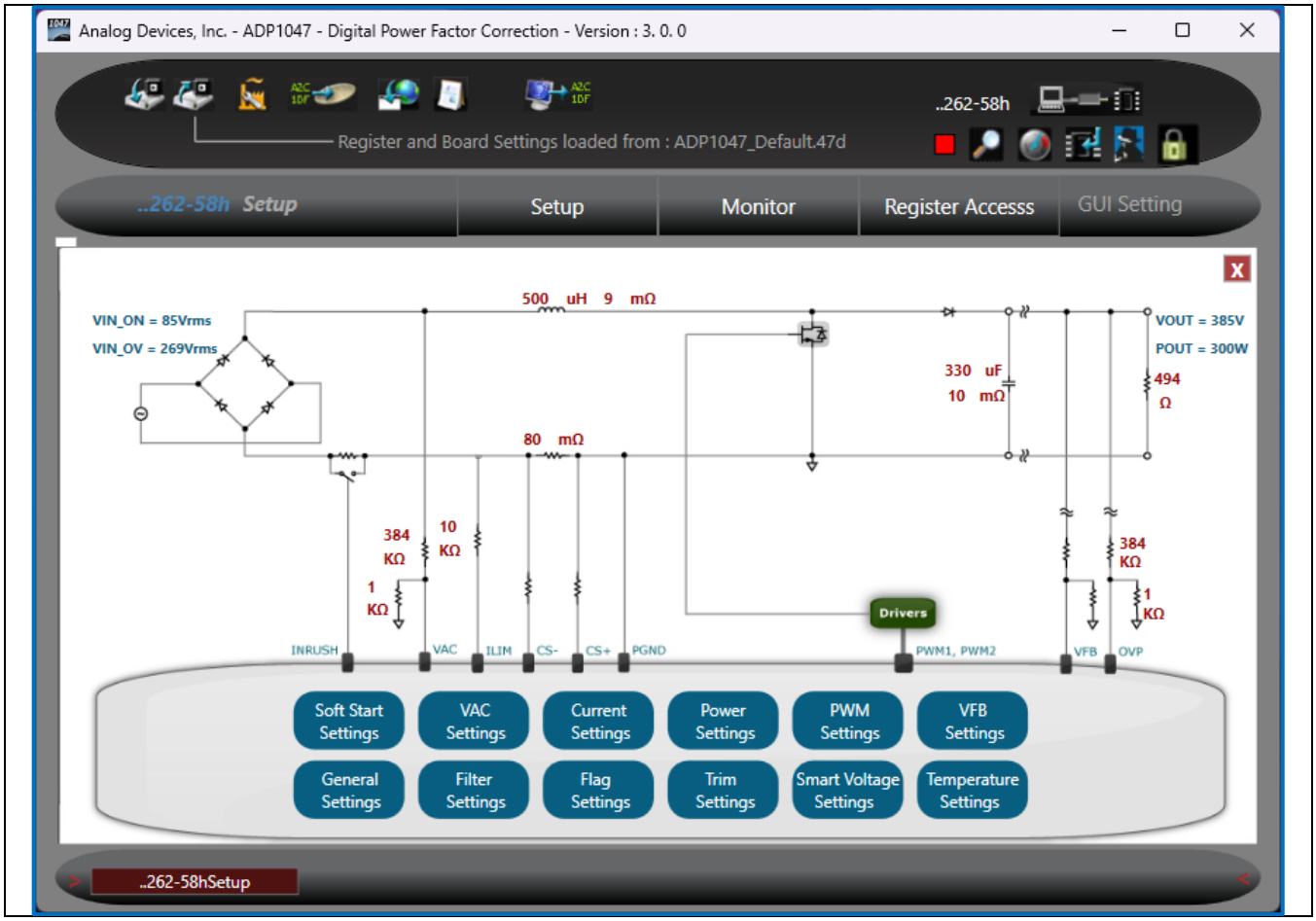

Figure 1. GUI Main Interface Window

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

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GUI CONTROLS

Link

Figure 2. Link Navigation

Table 1. Figure 2 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	USB to I2C Interface Number				Shows the last three digits of the ***USB to I2C Interface*** connected to ADP1047/ADP1048. This number is physically printed on the **USB to I2C Interface**.
2	ADP ADP1047/ ADP1048 Address				Shows to which address of the ADP1047/ADP1048 the GUI is connected.
3	Communication Link				Shows whether the GUI is communicating with the ADP1047/ADP1048.
4	PSON Status Indicator				Indicates the state of PSON operation command; red = off, green = on.
5	Scan				Scans for all ADP1047/ADP1048 devices connected to the computer. This function helps connect and disconnect devices once the GUI is running.
6	Dashboard				Opens the ***Dashboard*** window.
7	Update EEPROM	0xD5 0xFE81 0x15	[7:0] [6]	W RO W	Writes the contents of the registers to the EEPROM of ADP1047/ADP1048. This is accomplished by writing password twice to register 0xD5 (default is 0h) to unlock the EEPROM. The unlocking status can be checked by reading register 0xFE81 bit 6, which is followed by issuing a 0x15 command to write the contents to the EEPROM. Wait 40ms, then lock the EEPROM by writing any byte other than the password on register 0xD5.
8	Spy				Opens the ***Spy*** window.
9	Lock/Unlock	0xD6 0xFE37	[7:0] [7:0]	W R/W	Locks or unlocks write access for Trim registers.

Structural Navigation

Figure 3. Structural Navigation

Table 2. Figure 3 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Device Window Info				Shows the device address and the name of the window that is currently open.
2	Structural Navigation				If only one device is connected to the GUI, clicking the buttons opens the respective windows. If multiple devices are connected, clicking the buttons opens the window for the device selected in the *Link* section.

Windows Navigation

Figure 4. Windows Navigation

Table 3. Figure 4 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Arrows				Moves the tabs in their respective directions.
2	Tabs				Opens the window on whose name and device address is displayed.

Tools

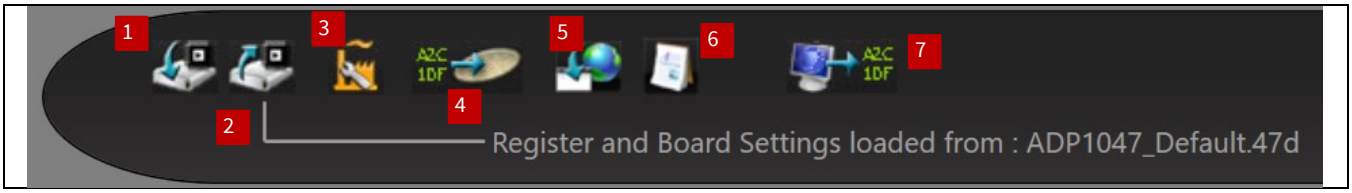

Figure 5. Tools Navigation

Table 4. Figure 5 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Save Register and Board Settings				Saves the contents of the register map and the board settings (external components) from the device selected in the *Link* section to either a ***.47d*** file or a ***.48d*** file.
2	Load Register and Board Settings				Loads the contents of the register map and the board settings (external components) to the device selected in the *Link* section from either a ***.47d*** file or a ***.48d*** file.
3	Load Factory-Trim Values				Loads the factory trim settings to the part.
4	EEPROM Access				Opens a page to access pages 4 to 15 of the EEPROM. These pages can be used to save any user-defined information.
5	Update GUI				Connects to Analog Devices and redirects to the page that contains the latest version of the GUI.
6	Reference Guide				Opens the GUI Reference Guide.
7	Generate HEX File				Generates a HEX file of the register map for use in a production environment.

Dashboard

Figure 6. Dashboard Navigation

Table 5. Figure 6 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	PS ON	0x01	[7]	R/W	Sets the device response to the operation command.
2	IPV	0x88	[15:0]	R	Displays the input voltage (V) in VIN linear mode format.
3	IPP	0x89	[15:0]	R	Displays the input current (A) in current linear mode format.
4	OPV	0x97	[15:0]	R	Displays the input power (W) in power linear mode format.
5	VOUT OV	0x7A	[7]	R	Red = The output voltage is above the OUT_OV_FAULT_LIMIT.
6	VIN UV	0x78	[3]	R	Red = General input undervoltage fault.
7	IIN OC	0xFE99	[2]	R	Red = The input current measured on the CS ADC is larger than the value in IIN_OC_FAULT_LIMIT.

SETUP

Main (ADP1047 Only)

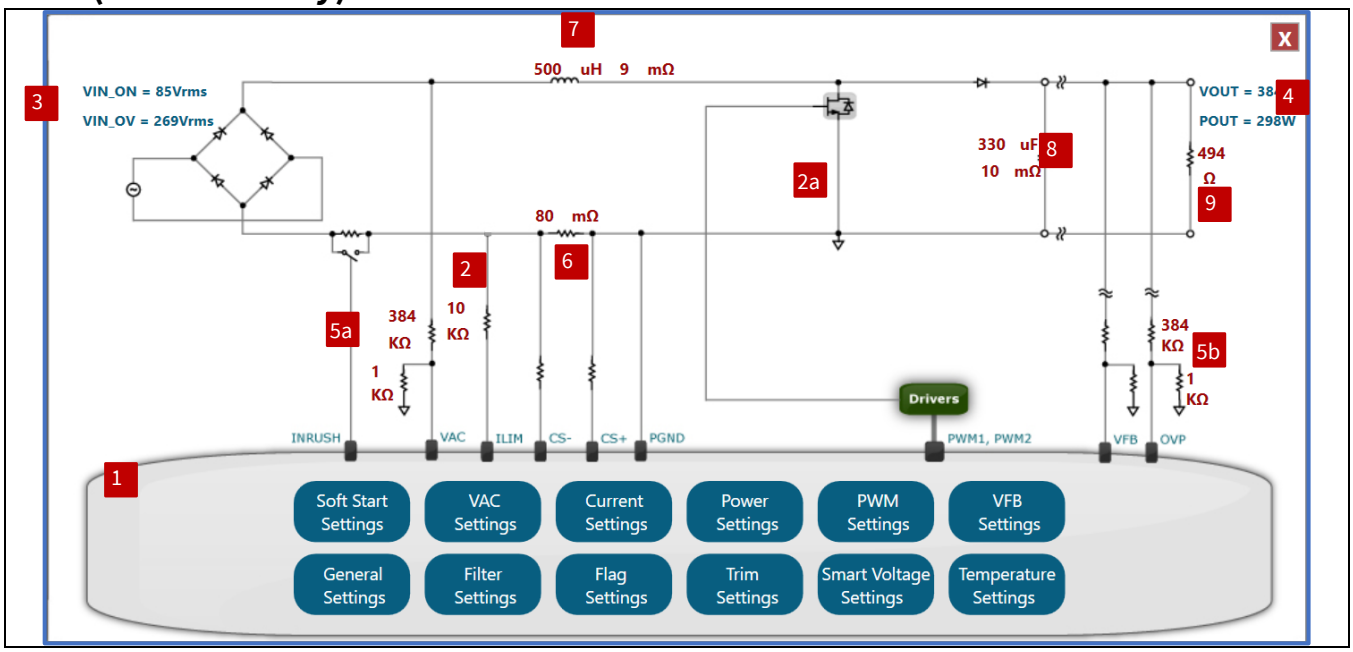

Figure 7. Single-Phase PFC

Table 6. Figure 7 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	ADP1047 Setup Blocks				The grey block represents the ADP1047, and the blue blocks represent the various setup blocks of the ADP1047. Click the blue blocks to open the settings for the corresponding windows. The components outside the ADP1047 represents the simplified power diagram connections needed for PFC operation and loop-compensation calculations.
2 2a	ILIM (Fast OC) Setting Source Resistor	0xFE3E	[7]	R/W	Sets the fast overcurrent ILIM setting either from the sense resistor [6] (negative level shifting current source) or source resistor [2a] (positive level shifting current source). Together with the ILIM resistor value, the fast OC level can be set accordingly in the ***Current Settings*** block.
3	Input Parameters	0x35 0x55	[16] [16]	R/W R/W	VIN_ON (AC turn on voltage) and VIN_OV (AC overvoltage level) are shown to provide the designed input operating range the PFC circuit. Use the ***VAC Settings*** block to update these parameters.

4	Output Parameters	0x21	[16]	R/W	VOUT (output voltage) and POUT (output power) are shown to provide a quick reference on the designed nominal output voltage and power of the PFC circuit. Use the ***VFB Settings*** block to configure the VOUT. Update POUT with the load resistor [9].
5a 5b	Input Voltage Divider Output Voltage Divider				External resistor dividers are needed to bring the input and output signals to the operating range of the ADC (0V to 1.6V). The default values ratio of 384kΩ and 1kΩ provide ~1V on the input pins VAC, VFB, and OVP, which work in most application in the < 500V range.
6	Current-Sense Resistor				Controls, protects, and monitors the PFC stage.
7	Inductor				Sets the value of the PFC inductor and the DCR value. Use the loaded inductance value for more accurate loop compensation.
8	Output Bulk Capacitors				Sets the value of the output bulk capacitors and the ESR value. The capacitor value is based on the hold-up time requirement.
9	Load Resistor				Set the equivalent resistance value for the nominal power rating (e.g., POUT = $VOUT^2/R_{LOAD}$).

Main (ADP1048 Only)

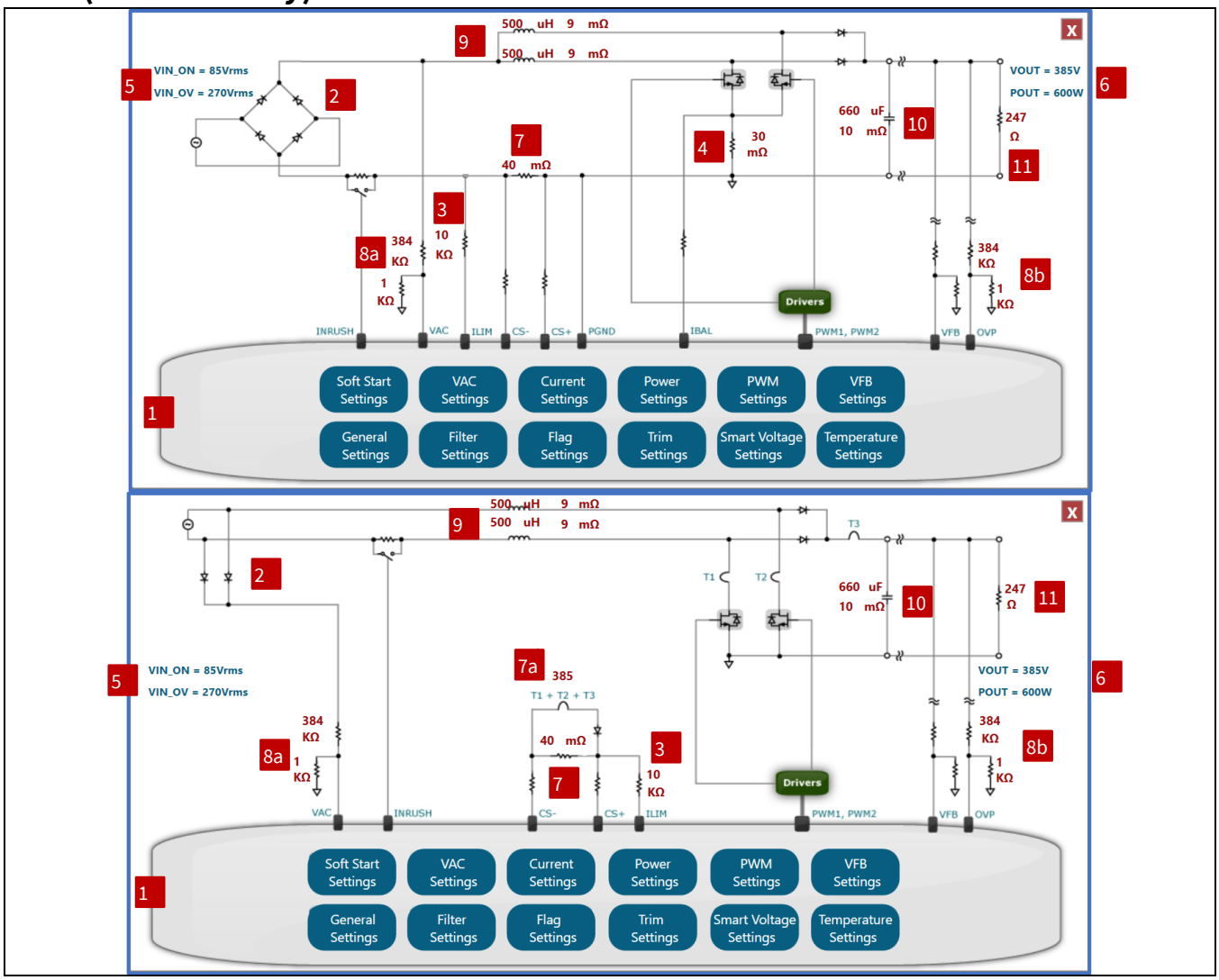

Figure 8. Interleaved PFC (Top) and Bridgeless PFC (Bottom)

Table 7. Figure 8 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	ADP1048 Setup Blocks				The grey block represents ADP1048 and the blue blocks represent the various setup blocks of the ADP1048. These blue blocks can be clicked to open the corresponding windows for settings. The components outside ADP1048 represents the simplified power diagram connection needed for PFC operation and loop-compensation calculations.
2	ADP1048 Operation	0xFE14	[4]	R/W	Sets either interleaved PFC operation (first diagram) or bridgeless PFC operation (second diagram).

3	ILIM (Fast OC) Setting	0xFE3E	[7]	R/W	Sets the fast overcurrent ILIM setting. For interleaved PFC, connect ILIM to either the sense resistor [7] or the source resistor [4]. For bridgeless PFC, connect through the current transformer sense resistor [7] for ground isolation. Together with the ILIM resistor value, use the ***Current Settings*** block to set the fast OC level accordingly.
4	IBAL Pin/ Source Resistor				For interleaved PFC operation, the source resistor connected to the IBAL pin is also used in maintaining current balance between the interleaved phases. For bridgeless PFC operation, use the IBAL pin to detect zero-crossing to synchronize the active power rail to the AC line phase.
5	Input Parameters	0x35 0x55	[16] [16]	R/W R/W	VIN_ON (AC turn on voltage) and VIN_OV (AC overvoltage level) are shown to provide the designed input operating range the PFC circuit. Use the ***VAC Settings*** block to update these parameters.
6	Output Parameters	0x21	[16]	R/W	VOUT (output voltage) and POUT (output power) are shown to provide a quick reference on the designed nominal output voltage and power of the PFC circuit. Configure VOUT on the ***VFB Settings*** block. Update POUT with the load resistor [11].
7 7a	Current-Sense Resistor Current-Sense Transformers				The current-sense resistor is used for control, protection, and monitoring of the PFC stage. For bridgeless PFC operation, use current transformers to simplify the sensing and to minimize power dissipation.
8a 8b	Input Voltage Divider Output Voltage Divider				External resistor dividers are needed to bring the input and output signals within the operating range of the ADC (0V to 1.6V). The default values ratio of 384kΩ and 1kΩ provide ~1V on the input pins VAC, VFB, and OVP. They work in most application in < 500V range.
9	Inductors				Sets the value of the PFC inductors and the DCR values. Use the loaded inductance value for more accurate loop compensation.
10	Output Bulk Capacitors				Sets the value of the output bulk capacitors and the ESR value. The capacitor value is based on the hold-up time requirement.
11	Load Resistor				Sets the equivalent resistance value for the nominal power rating (e.g., POUT = $VOUT^2/R_{LOAD}$).

Soft-Start Settings

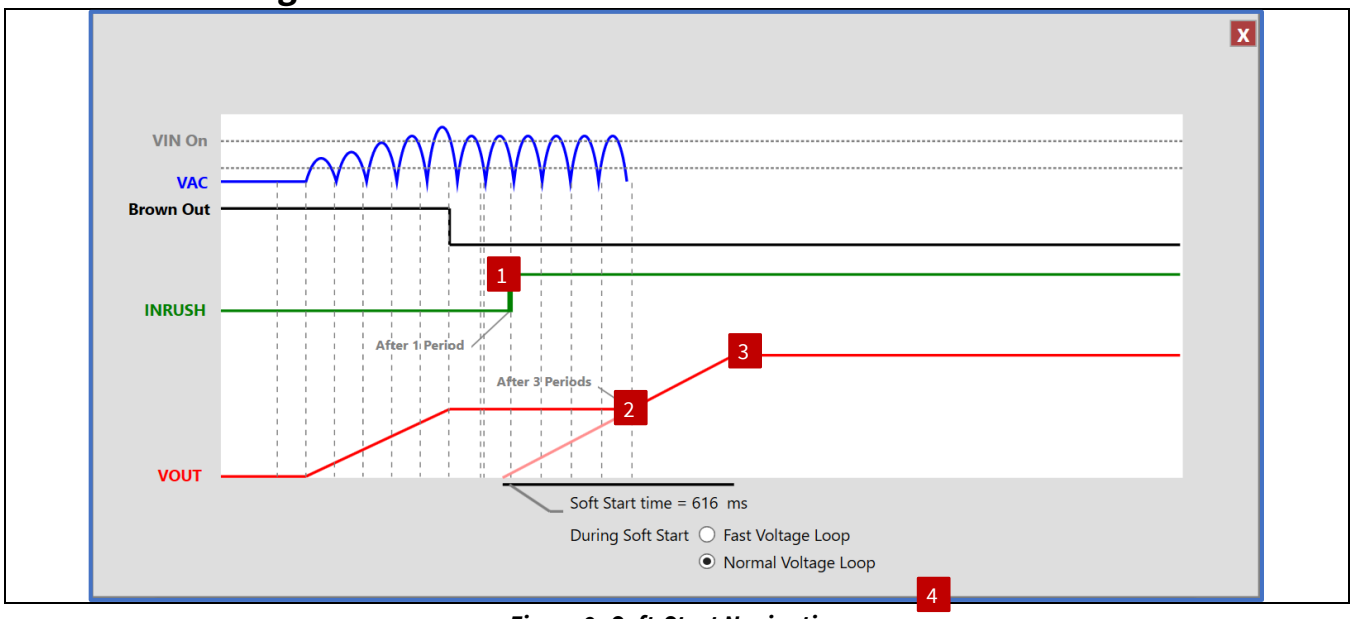

Figure 9. Soft-Start Navigation

Table 8. Figure 9 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Inrush Delay	0xFE2E	[2:0]	R/W	Sets the inrush signal delay time after the BROWN_OUT flag goes low (0 to 7 AC cycles after brownout). Delay time allows the output bulk capacitor to charge to peak AC voltage through the NTC/PTC inrush resistor.
2	Soft-Start Delay Time	0xFE2D	[5:3]	R/W	Sets the delay time between the inrush signal and the origin of the soft start (0 to 7 AC cycles after brownout).
3	Sof-Start Time	0xFE2D	[2:0]	R/W	Sets the ramp-up time of the output: 112ms, 168ms 224ms, 280ms, 392ms, 504ms, 616ms, 728ms
4	Enable Fast Loop during Soft Start	0xFE24	[1]	R/W	Enables either ***Fast Voltage Loop*** or ***Normal Voltage Loop*** by clicking one of the buttons.

VAC Settings

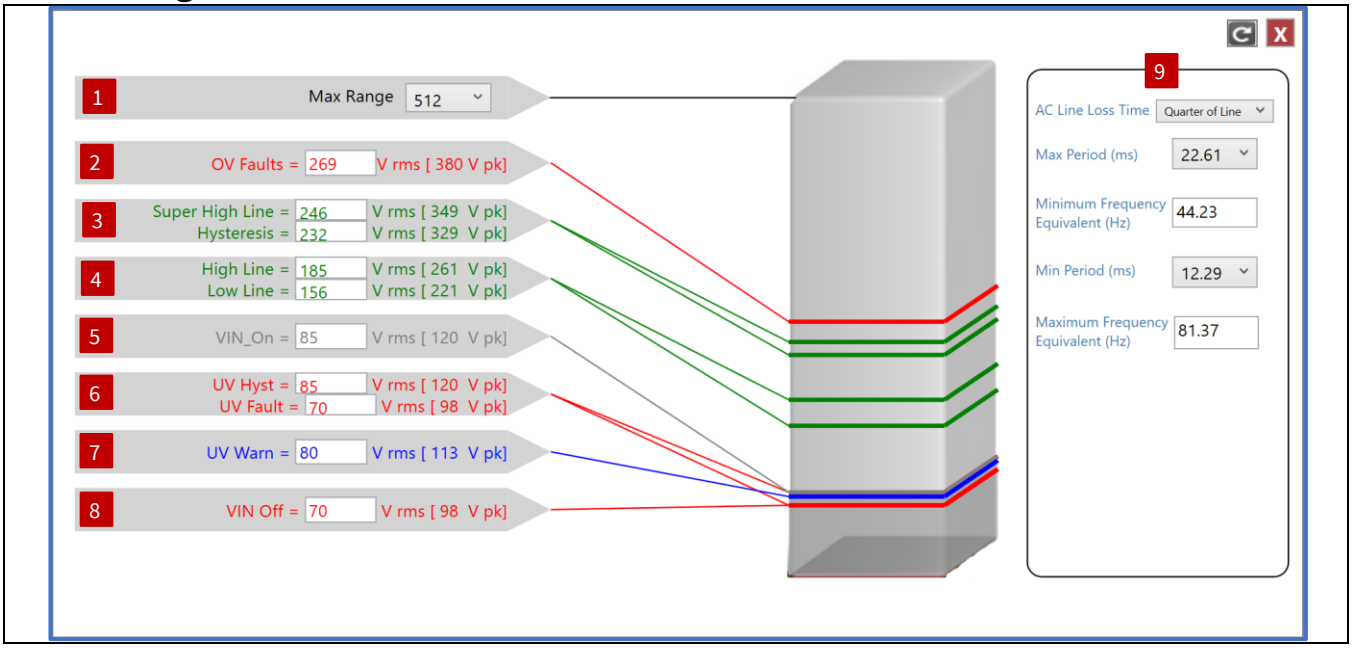

Figure 10. VAC Settings Navigation

Table 9. Figure 10 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range	0xFE39	[5:3]	R/W	This sets the exponent for the input voltage. Supported Max Range are 256, 512, and 1024.
		0x55	[15:0]	R/W	The voltage value in RMS is calculated using the linear mode format V = Y * 2^N, where Y is the mantissa using the lower 11 bits [10:0] and N is the 2-s complement of the upper 3 bits [13:11].
		0x35	[15:0]	R/W	
		0x36	[15:0]	R/W	
		0x58	[15:0]	R/W	
		0x59	[15:0]	R/W	
2	OV Fault Exponent N	0x55	[13:11]	R	Sets the upper volt measured at the PFC input voltage that causes an overvoltage fault condition.
	Mantissa		[10:0]	R/W	To set the value, either directly input the value or use the slider. Press ***Enter*** to confirm value change.
3	Super High Line	0xFE4B	[10:0]	R/W	Sets the input voltage value as a super high line limit for smart output voltage feature. Register value is ~6.65 * V_{RMS}
	Hysteresis	0xFE4D	[7:0]	R/W	This sets the voltage hysteresis of the super high line voltage for the smart output voltage operation. The voltage delta is limited to 38V. Register value is ~ (SuperHighLine-Hysteresis)V_{RMS} * 6.65.

4	High Line Low Line	0xFE35 0xFE36	[7:0] [7:0]	R/W R/W	This sets the high line limit. When the input voltage is higher than this value, the current loop filter for high line input is used. Register value is ~V_{RMS}/2.40. This sets the low line limit. When the input voltage is lower than this value, the current loop filter for low input is used. Register value is ~V_{RMS}/2.40.
5	VIN On Exponent N Mantissa	0x35	[13:11] [10:0]	R R/W	Sets the value of the input voltage to start power conversion.
6	UV Fault Exponent N Mantissa UV Hysteresis	0x59 0xFE51	[13:11] [10:0] [7:0]	R R/W R/W	Sets the upper voltage measured at the PFC input voltage that causes an undervoltage fault condition. Register value is ~(UV Hysteresis – UV Fault)V_{RMS} * 4.0.
7	UV Warn Exponent N Mantissa	0x58	[13:11] [10:0]	R R/W	Sets the upper voltage measured at the PFC voltage that causes an undervoltage warning condition.
8	VIN Off Exponent N Mantissa	0x36	[13:11] [10:0]	R R/W	Sets the value of the input voltage to stop power conversion.
9	AC Line Loss Time Max Period Min Period	0xFE2E 0xFE28 0xFE27	[4:3] [7:0] [7:0]	R/W R/W R/W	Sets the timer for the VIN_LOW_FLAG measurement. Sets the maximum AC line period of the input voltage. Equivalent frequency is listed for easy reference. Sets the minimum AC line period of the input voltage. Equivalent frequency is listed for easy reference.

Current Settings

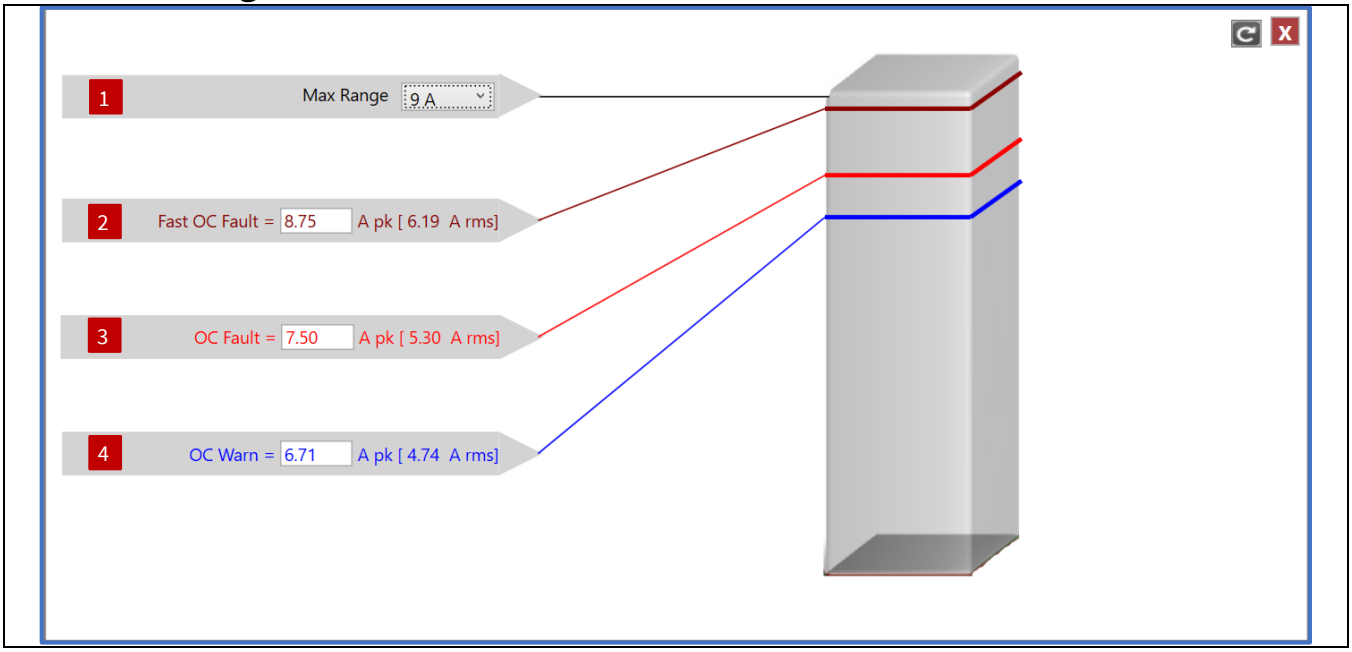

Figure 11. Current Settings Navigation

Table 10. Figure 11 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range	0xFE39 0x5B 0x5D 0xFE3E	[10:6] [15:0] [15:0] [6:5]	R/W R/W R/W R/W	Sets the exponent for the input current. The drop-down menu provides two ranges that correspond to the current-sense ADC voltage ranges: V_{ADC} = 500mV or 750mV rounded off. Max Range = V_{ADC}/Current-Sense Resistor Current-Sense Resistor: See Table 6, item 6.
2	Fast OC Fault	0xFE3E	[6:5]	R/W	Sets the ILIM absolute value. The value is determined by the discrete ILIM current value and the ILIM resistor. See Table 6, item 2. To set the value, either directly input the value or use the slider. Press ***Enter*** to confirm the value change.
3	OC Fault Exponent N Mantissa	0x5B	[15:11] [10:0]	R R/W	Sets the accurate overcurrent threshold measured at the PFC input current that causes an overcurrent fault condition. Current value in RMS is calculated using the linear mode format ($I = Y * 2^N$), where Y is the mantissa that uses the lower 11 bits [10:0], and N is the 2-s complement of the upper 5 bits [15:11].
4	OC Warn Exponent N	0x5D	[15:11]	R	Sets the accurate overcurrent threshold measured at the PFC input current that causes an overcurrent warning condition.

	Mantissa		[10:0]	R/W	Value stored is in RMS.

Power Settings (ADP1047 Only)

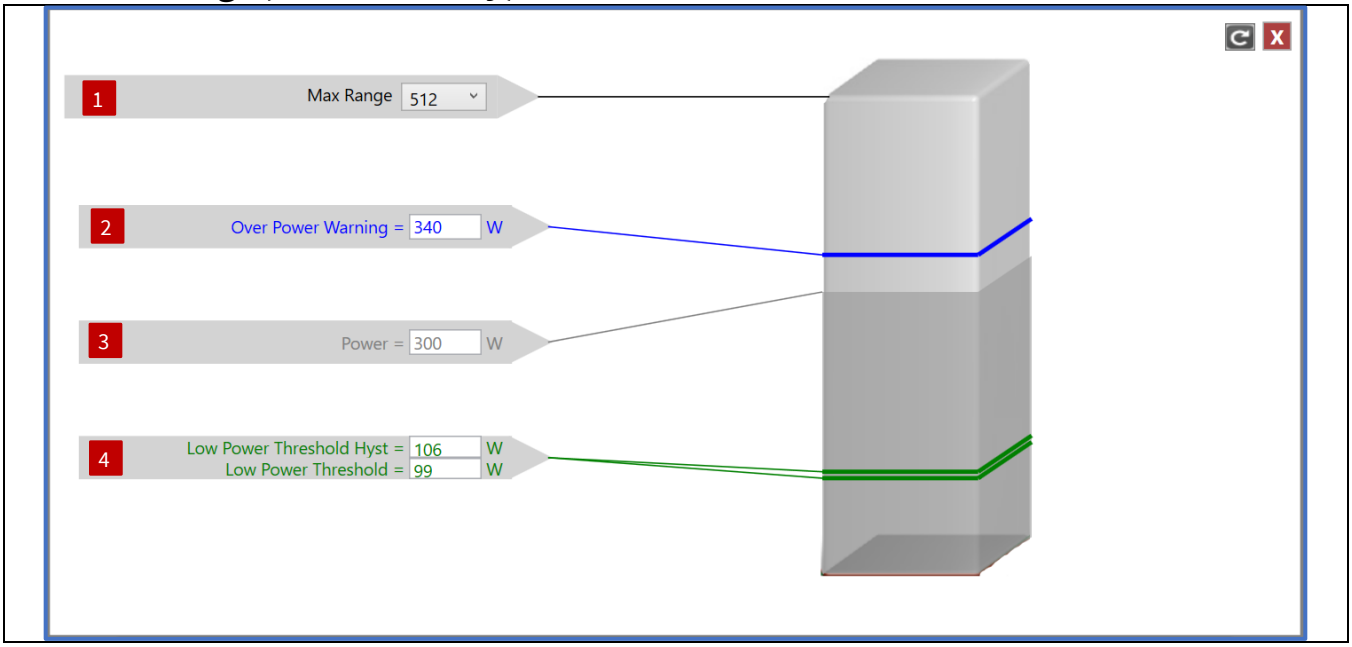

Figure 12. Power Settings (ADP1047 Only) Navigation

Table 11. Figure 12 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range	0xFE39 0x6B 0xFE32 0xFE4E	[2:0] [15:0] [7:0] [7:0]	R/W R/W R/W R/W	Sets the exponent for the input power. Supported Max Range values are 256, 512, 1024, up to 32768. Before changing this setting, ensure the other values are less than the new Max Range value selected, otherwise, the change will not be applied, and a warning message will be displayed.
2	Over-Power Warning Exponent N Mantissa	0x6B	[13:11] [10:0]	R R/W	Sets the value of the input power, in watts, which triggers a warning that the input power is high. The power value in watts is calculated using the linear mode format ($P = Y * 2^N$) , where Y is the mantissa that uses the lower 11 bits [10:0], and N is the 2-s complement of the upper 3 bits [13:11]. To set the value, either directly input the value or use the slider. Press ***Enter*** to confirm value change.
3	Power				This is the nominal output power of the PFC displayed for quick reference compared to other parameters.

					Configure this value through the load resistor, R_{LOAD},on the main page. See Table 6, item 11, and VOUT in the ***VFB Settings*** (e.g., POUT = $VOUT^2/R_{LOAD}$).
4	Low-Power Threshold Hyster	0xFE4E	[7:0]	R/W	Sets the power hysteresis for low power mode operation. The register value is the ~PowerDelta/1.4, (e.g., 7/1.4).
	Low Power Threshold	0xFE32	[7:0]	R/W	Sets threshold value of the lower power operation detection. Register value is ~Power/1.4, e.g., 106/1.4.

Power Settings (ADP1048 Only)

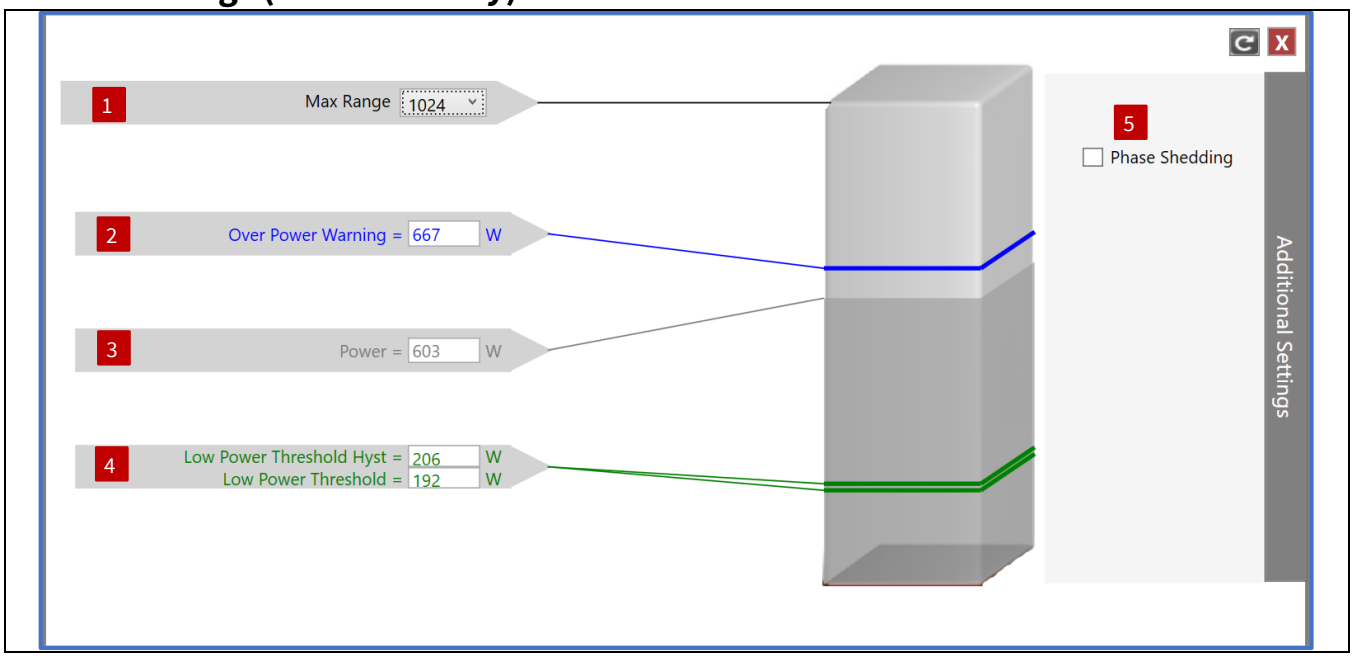

Figure 13. Power Settings (ADP1048 Only) Navigation

Table 12. Figure 13 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range	0xFE39 0x6B 0xFE32 0xFE4E	[2:0] [15:11] [10:0] [7:0]	R/W R/W R/W R/W	Sets the exponent for the input power. Supported Max Range values are 256, 512, 1024, up to 32768. Before changing this setting, ensure the other values are less than the new Max Range value selected, otherwise, the change will not be applied, and a warning message will be displayed.
2	Over-Power Warning Exponent N Mantissa	0x6B	[13:11] [10:0]	R R/W	Sets the value of the input power, in watts, which triggers a warning that the input power is high. To set the value, either directly input the value or use the slider. Press ***Enter*** to confirm value change.

3	Power				This is the nominal output power of the PFC displayed for quick reference compared to other parameters. Configure this value through the load resistor, R_{LOAD}, on the main page. See Table 6, item 11, and VOUT in the ***VFB Settings*** (e.g., POUT = $VOUT^2/R_{LOAD}$).
4	Low-Power Threshold Hyst Low-Power Threshold	0xFE4E 0xFE32	[7:0] [7:0]	R/W R/W	Sets the power hysteresis for low-power mode operation. The register value is the ~PowerDelta/2.8, (e.g., 14/2.8). This sets the threshold value of the lower power operation detection. The register value is ~Power/2.8 (e.g., 192/2.8).
5	Phase Shedding	0xFE4F	[4]	R/W	Enables or disables phase shedding for interleaved PFC to achieve higher efficiency at lower output power. This feature is not available in bridgeless PFC mode.

PWM Settings (ADP1047 Only)

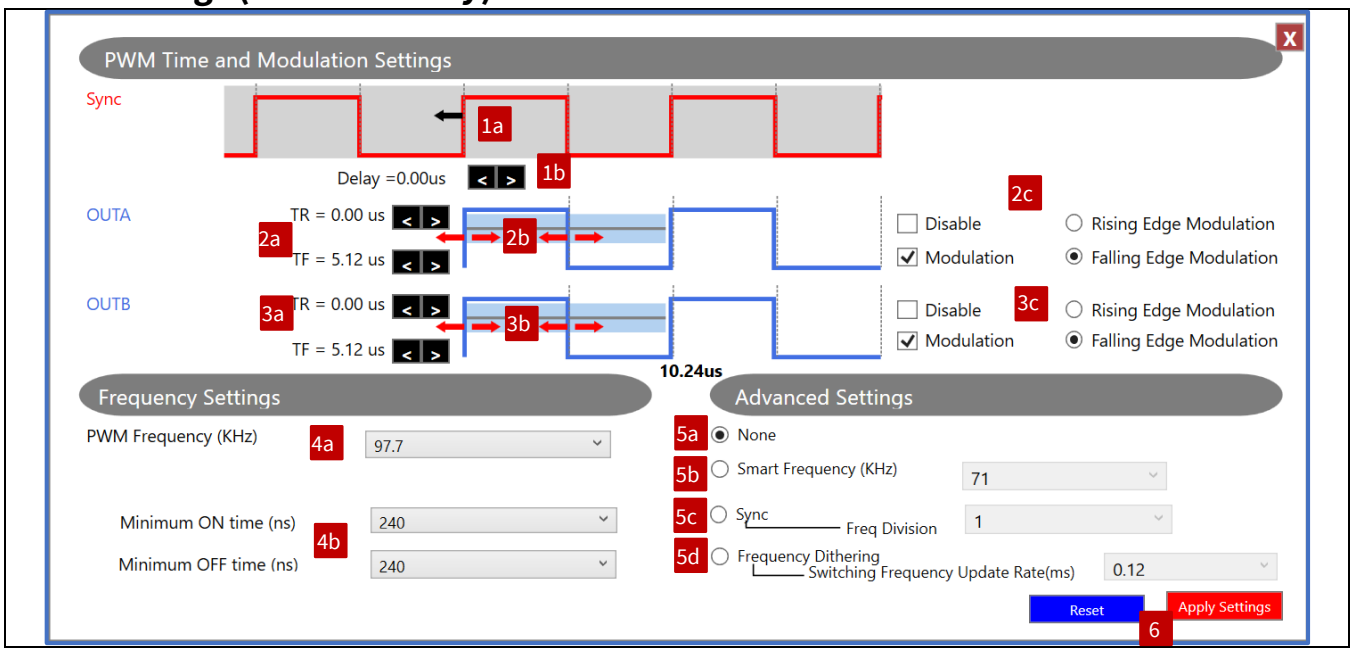

Figure 14. PWM Settings (ADP1047 Only) Navigation

Table 13. Figure 14 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1a 1b	Sync Delay - Slider - Buttons	0xFE4C	[15:0]	R/W	Sets the additional delay of the synchronization reference clock to the rising edge of PWM. Adjustments can be made using the slider [1a] for coarser steps or using buttons [1b] for finer adjustment. Step size is 40ns, and value is clamped to 112.5% of the programmed frequency. If desired, enable the synchronization feature in the advanced settings [5c].
2a 2b 2c	OUTA (PWM) - Buttons - Sliders - Configurations	0xFE0C 0xFE0D 0xFE0E 0xFE0F 0xFE14	[7:0] [3:2] [7:0] [3:2] [2:1]	R/W R/W R/W R/W R/W	Main PWM OUTA for driving a PFC MOSFET. Adjust both the rising (t1) and falling (t2) PWM edges using buttons [2a] for precise 40ns adjustments or using sliders [2b] for coarser steps. Enable or disable the PWM, enable or disable the modulation, and select either leading edge or trailing edge modulation scheme.
3a 3b 3c	OUTB (PWM2) - Buttons - Sliders - Configuration	0xFE10 0xFE11 0xFE12 0xFE13 0xFE14	[7:0] [3:2] [7:0] [3:2] [2:1]	R/W R/W R/W R/W R/W	Drives active snubber circuit for a zero-voltage transition, soft-switched PFC circuit. Adjust both rising (t1) and falling (t2) PWM edges using buttons [2a] for precise 40ns adjustment or using sliders [2b] for coarser steps.

					Enable or disable the PWM, enable or disable the modulation, and select either leading edge or trailing edge modulation scheme.
	Frequency Settings	0xFE1B			
4a	PWM Frequency	0xFE15	[5:0]	R/W	Sets the switching frequency between 30kHz to 400kHz.
4b	Minimum On Time		[7:4]	R/W	Sets the minimum on time in 80ns steps from 0ns to 1.2µs.
	Minimum Off Time		[3:0]	R/W	Sets the minimum off time in 80ns steps from 40ns to 1.2µs.
	Advanced Settings	0xFE4F	[7:0]	R/W	Advanced feature configuration
5a	None				No advanced feature is enabled.
5b	Smart Frequency	0xFE4F	[3]	R/W	Enables smart frequency switching at lower loads to achieve higher efficiency. The frequency value must be lower than PWM frequency.
	-Frequency Select	0xFE1C	[5:0]	R/W	
5c	Synchronization	0xFE4F	[1]	R/W	Enables PWM synchronization (f_{SW}) with external clock source (f_{SYNC}).
		0xFE1E	[1:0]	R/W	
5d	- Freq Division		[0]	R/W	Frequency division sets the ratio between f_{SW} and f_{SYNC}.
	Frequency Dithering	0xFE4F	[6:0]	R/W	Enables frequency dithering for EMI reduction, which varies the switching period by ~±12.5%.
	- Switching Frequency Update Rate	0xFE1D			This sets the period for updating the switching frequency in 40µs steps.
6	Reset				Undoes uncommitted changes in simulation mode. If connected to a device, it reloads the programmed settings.
	Apply Settings				This button applies all the PWM settings to the part.

PWM Settings (ADP1048 Only)

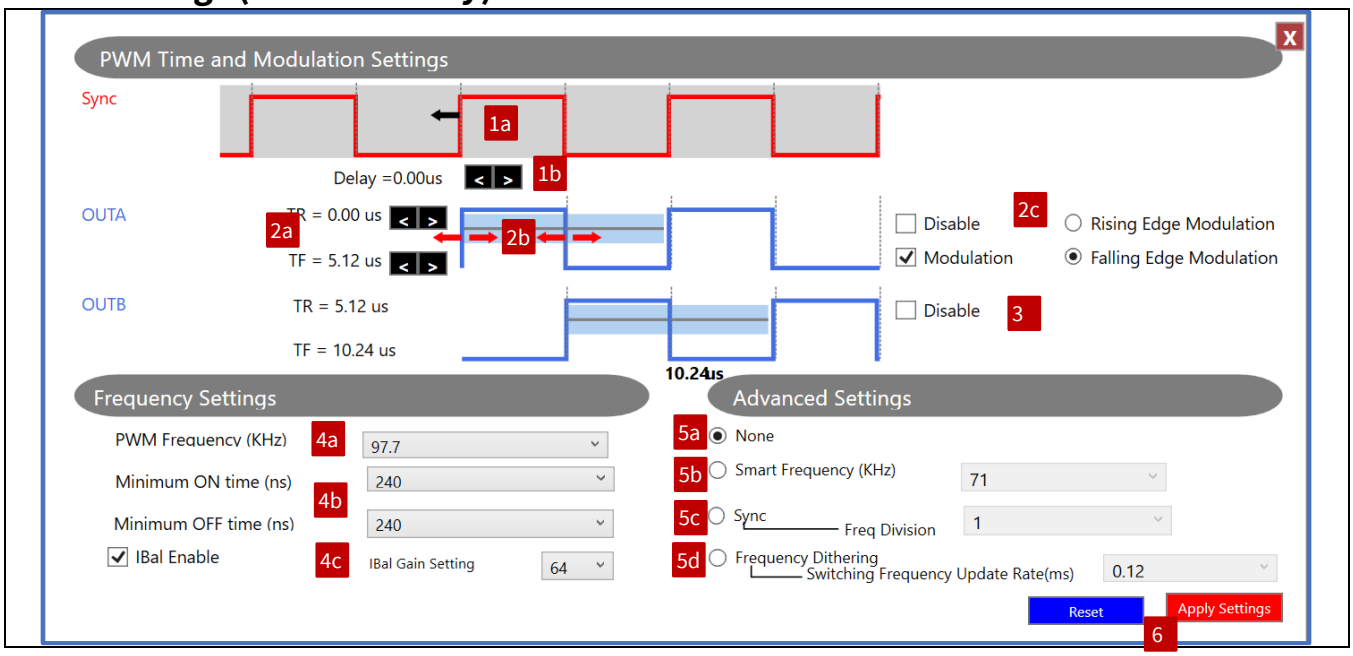

Figure 15. PWM Settings (ADP1048 Only) Navigation

Table 14. Figure 15 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1a 1b	Sync Delay - Slider - Buttons	0xFE4C	[15:0]	R/W	Sets the additional delay of the synchronization reference clock to the rising edge of PWM. Use the slider [1a] for coarser steps or use the buttons [1b] for finer adjustment. The step size is 40ns and the value is clamped to 112.5% of the programmed frequency. If desired, enable the synchronization feature in the advanced settings [5c].
2a 2b 2c	OUTA (PWM) - Buttons - Sliders - Configurations	0xFE0C 0xFE0D 0xFE0E 0xFE0F 0xFE14	[7:0] [3:2] [7:0] [3:2] [2:1]	R/W R/W R/W R/W R/W	Drives PFC MOSFET. Adjust both rising (t1) and falling (t2) PWM edges by using buttons [2a] for precise 40ns adjustments or using the sliders [2b] for coarser steps. Enable or disable the PWM, enable or disable the modulation, and select either leading edge or trailing edge modulation scheme.
3	OUTB (PWM2) - Configuration	0xFE10 0xFE11 0xFE12 0xFE13 0xFE14	[7:0] [3:2] [7:0] [3:2] [2:1]	R/W R/W R/W R/W R/W	Interleaved PWM2 OUTB for driving MOSFET of the other PFC phase. For the ADP1048, PWM2 is automatically configured to be 180° out of phase for interleaved and in-phase for bridgeless in relation to OUTA.

					The only enable or disable option is available for OUTB in the ADP1048.
	Frequency Settings				
4a	PWM Frequency	0xFE1B	[5:0]	R/W	Sets the switching frequency between 30kHz to 400kHz.
4b	Minimum On-Time	0xFE15	[7:4]	R/W	Sets the minimum on-time in 80ns steps from 0ns to 1.2µs.
4c	Minimum Off-Time	0xFE43	[3:0]	R/W	Sets the minimum off-time in 80ns steps from 40ns to 1.2µs.
	IBAL Configuration		[7:0]	R/W	The ADP1048 provides a current balancing circuit for interleaved PFC or AC-line phase detection for bridgeless. The IBAL feature is enabled by default and disabled only for specific debugging purposes. The IBAL gain can be set from 0 to 127.
	Advanced Settings	0xFE4F	[7:0]	R/W	Advanced Feature Configuration
5a	None				No advanced feature is enabled.
5b	Smart Frequency -Frequency Select	0xFE4F 0xFE1C	[3] [5:0]	R/W R/W	Enables smart frequency switching at lower loads to achieve higher efficiency. The frequency value must be lower than PWM frequency.
5c	Synchronization - Freq Division	0xFE4F 0xFE1E	[1] [1:0]	R/W R/W	Enables PWM synchronization (f_{SW}) with an external clock source (f_{SYNC}). Frequency division sets the ratio between f_{SW} and f_{SYNC}.
5d	Frequency Dithering - Switching Frequency Update Rate	0xFE4F 0xFE1D	[0] [6:0]	R/W R/W	Enables frequency dithering for EMI reduction, which varies switching period by ~±12.5%. Sets the period for updating the switching frequency in 40µs steps.
6	Reset				Undoes uncommitted changes in simulation mode. If connected to a device, it reloads the programmed settings.
	Apply Settings				Applies all the PWM settings to the part.

VFB Settings

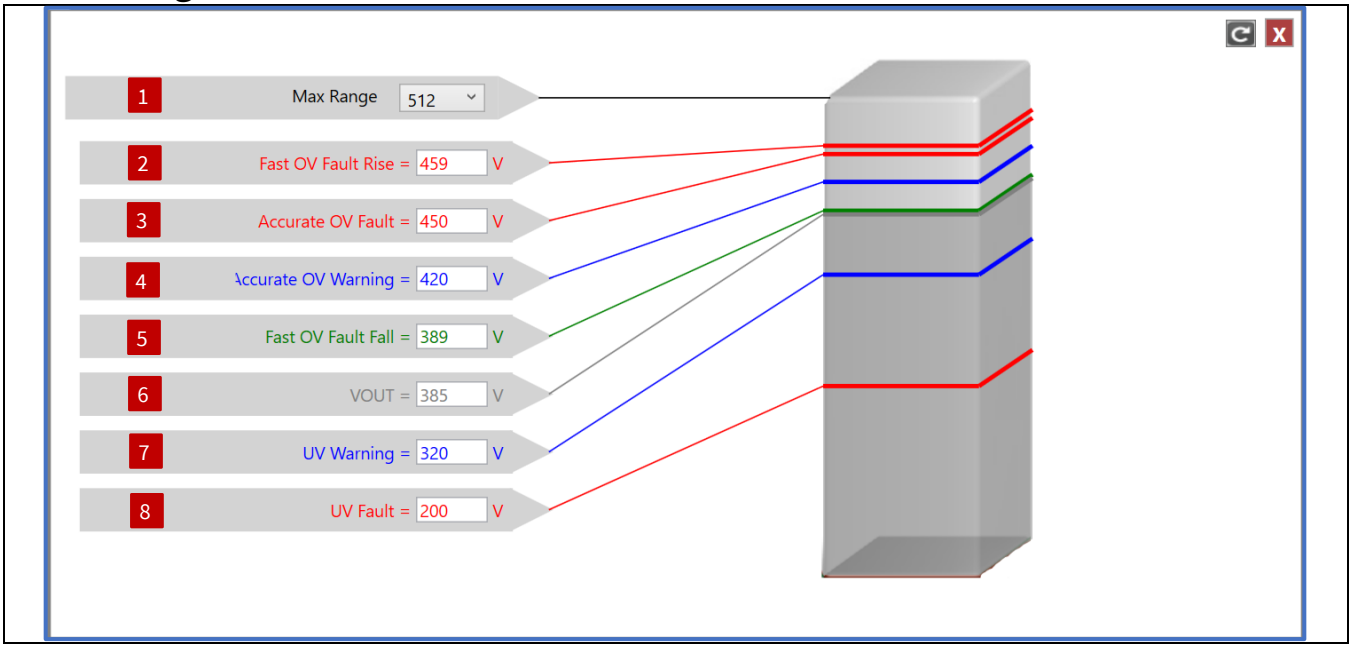

Figure 16. VFB Settings Navigation

Table 15. Figure 16 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range	0x20 0x21 0x40 0x42 0x44	[2:0] [11:0] [10:0] [10:0] [10:0]	R/W R/W R/W R/W R/W	Sets the exponent for the output voltage. Supported Max Range values are 256, 512, 1024, and 2048. Ensure all other values are less than the Max Range selected, otherwise a warning message will be displayed. The output voltage value is calculated using a linear mode format ($V = Y * 2^N$), where Y is the mantissa (lower bits), and N is the exponent in 2-s complement (upper bits or register 0x20).
2	Fast OV Fault Rise	0xFE2F	[6:0]	R/W	Sets the rising threshold of an analog comparator at the OVP pin input. Threshold OVP_{th} = (register value * 0.492/128) + 1. The equivalent voltage is based on OVP voltage divider, $V_{OVP} = OVP_{TH} * (1 + R_{UP}/R_{DOWN})$. The default divider ratio is 384kΩ and 1kΩ, the minimum setting is 385V, and the 0x3F register value is 478V. To set a value, directly input the value or use the slider. Press ***Enter*** to confirm value change.
3	Accurate OV Fault	0x20	[2:0]	R/W	

	Exponent N Mantissa Accurate OV Hyst Exponent N Mantissa	0x40 0x20 0xFE50	[10:0] [2:0] [7:0]	R/W R/W R/W	Sets the accurate overvoltage threshold measured at the PFC output, which triggers an overvoltage fault condition. Sets the hysteresis for VOUT_OV_FAULT condition. The register value is the difference between OV Fault and OV Hyst values . Hysteresis only applies when the disable output option is selected as VOUT_OV_FAULT_RESPONSE. See the *Flag Settings* section. The PFC output is enabled when the output voltage is lower than the VOUT_OV_LIMIT minus this hysteresis.
4	Accurate OV Warning Exponent N Mantissa	0x20 0x42	[2:0] [10:0]	R/W R/W	Sets the accurate overvoltage threshold measured at the PFC output that causes an overvoltage warn condition.
5	Fast OV Fault Fall	0xFE30	[6:0]	R/W	Similar to Fast OV Fault Rise, this sets the falling threshold of an analog comparator at the OVP pin input. Threshold OVP_{TH} = (register value * 0.492/128) + 1.
6	VOUT Exponent N Mantissa	0x20 0x21	[2:0] [11:0]	R/W R/W	Sets the VOUT to the commanded value.
7	UV Warning Exponent N Mantissa	0x20 0x43	[2:0] [10:0]	R/W R/W	Sets the accurate undervoltage threshold measured at the PFC output that triggers an undervoltage warning condition.
8	UV Fault Exponent N Mantissa	0x20 0x44	[2:0] [10:0]	R/W R/W	Sets the accurate undervoltage threshold measured at the PFC output that triggers an undervoltage fault condition.

General Settings

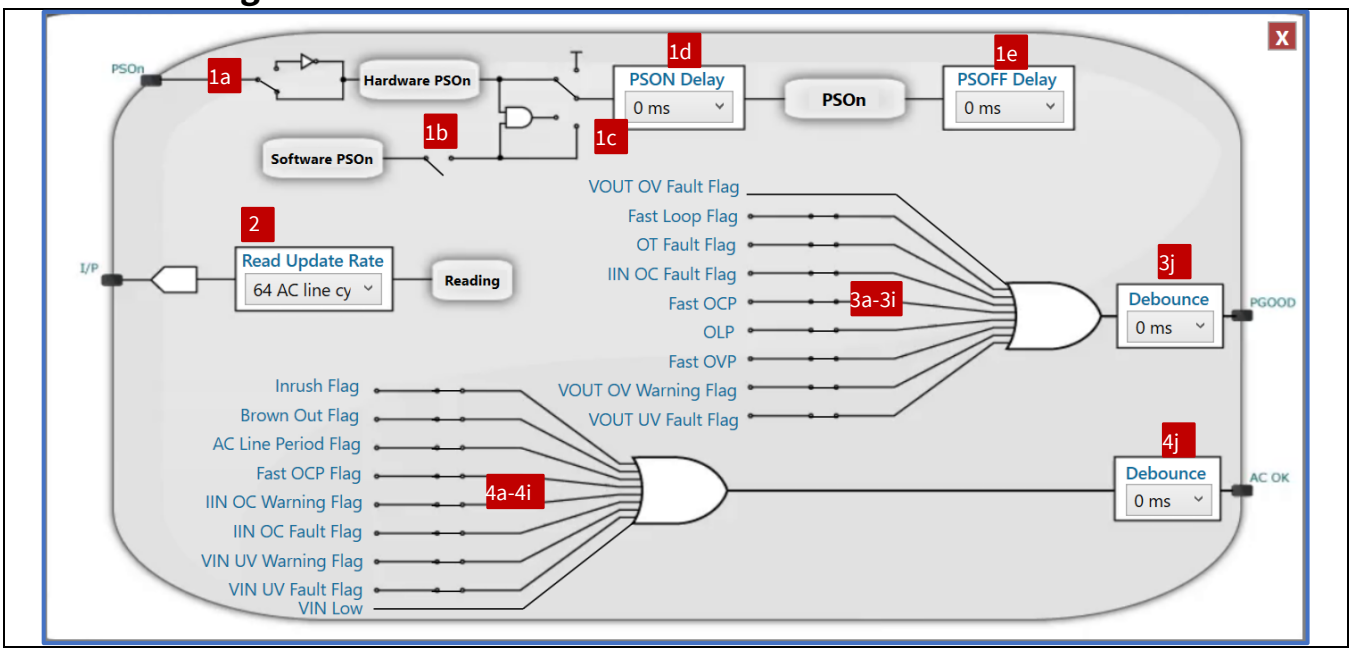

Figure 17. General Settings Navigation

Table 16. Figure 17 Callouts

NO.	NAME	REG	BITSs	R/W	DESCRIPTION
1a	PSON Settings Control Pin Polarity	0x02	[1]	R/W	Sets polarity for the control pin (PSON).
1b	Operation	0x01	[7]	R/W	Sets the device response to the operation command.
1c	PSON Configuration Power-Up Control	0x02	[4:2]	R/W	Set if the device powers up when power is present or wait for enable from the control pin and/or the OPERATION command.
1d	PSON Delay	0xFE06	[3:2]	R/W	Sets the time from when the PSON signal is set to when soft start begins: 0ms, 50ms, 250ms or 1s.
1e	PSOFF Delay	0xFE06	[1:0]	R/W	Sets the time from when the PSON signal is cleared to when device is turned off: 0ms, 50ms, 250ms, or 1s.
2	Read Update Rate	0xFE3A	[2:0]	R/W	Sets averaging window for the PWR current and voltage reading. The register value is in half AC cycles while GUI is specified in AC cycles for simplicity.

3a	PGOOD Config	0xFE0A	[7:0]	R/W	Specifies the flags that are checked to determine the PGOOD status.
3b	VOUT OV Fault Flag		[0]	R/W	VOUT OV Flag is always reflected on PGOOD status.
3c	Fast Loop Flag		[1]	R/W	If the switch is open, PGOOD ignores Fast Loop flag.
3d	OT Fault Flag		[2]	R/W	If the switch is open, PGOOD ignores Over Temperature Fault flag.
3e	IIN OC Fault Flag		[3]	R/W	If the switch is open, PGOOD ignores Input OverCurrent Fault flag.
3f	Fast OCP		[4]	R/W	If the switch is open, PGOOD ignores Fast OCP flag.
3g	OLP		[5]	R/W	If the switch is open, PGOOD ignores Open Loop flag.
3h	Fast OVP		[6]	R/W	If the switch is open, PGOOD ignores Fast OVP flag.
3i	VOUT OV Warning Flag	0xFE05	[7]	R/W	If the switch is open, PGOOD ignores VOUT OV Warning flag.
3j	VOUT UV Fault Flag		[3:0]	R/W	If the switch is open, PGOOD ignores VOUT UV Fault flag.
	PGOOD Debounce				Sets the debounce time for PGOOD pin: 0ms, 200ms, 320ms, or 600ms.
	ACOK Config	0xFE0B	[7:0]	R/W	Specifies which flags are checked to determine the ACOK status.
4a	Inrush Flag		[0]	R/W	If the switch is open, ACOK ignores Inrush flag.
4b	Brown Out Flag		[1]	R/W	If the switch is open, ACOK ignores Brown Out flag.
4c	AC Line Period Flag		[2]	R/W	If the switch is open, ACOK ignores AC Line Period flag.
4d	Fast OCP Flag		[3]	R/W	If the switch is open, ACOK ignores Fast OCP flag.
4e	IIN OC Warning Flag		[4]	R/W	If the switch is open, ACOK ignores Input OC Warning flag.

	I				
4f	IN OC Fault Flag		[5]	R/W	If the switch is open, ACOK ignores Input OC Fault flag.
4g	VIN UV Warning Flag		[6]	R/W	If the switch is open, ACOK ignores VIN UV Warning flag.
4h	VIN UV Fault Flag	0xFE05	[7]	R/W	If the switch is open, ACOK ignores the AC Line Period flag.
4i	VIN OFF				The VIN_OFF flag is always reflected in the ACOK status.
4j	ACOK Debounce		[7:4]	R/W	Sets the debounce time for the ACOK pin: 0ms, 200ms, 320ms, or 600ms.

Filter Settings

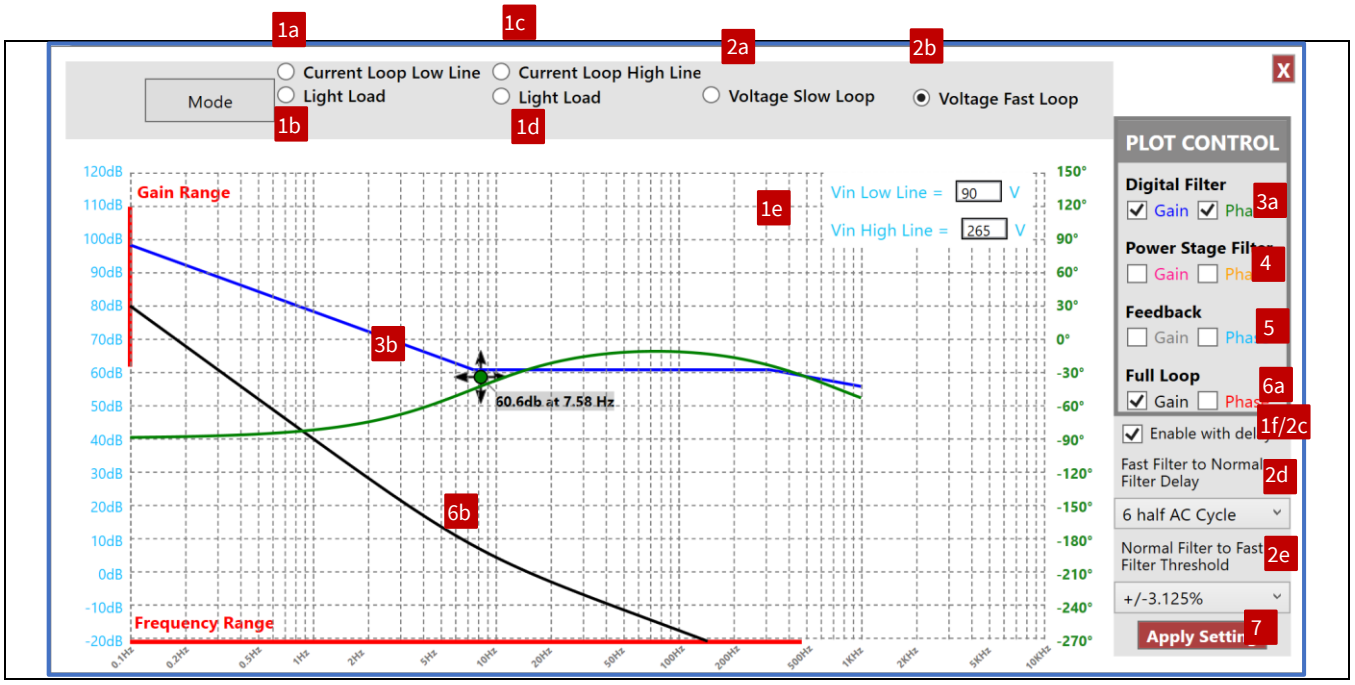

Figure 18. Filter Settings Navigation

Table 17. Figure 18 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
	Current-Loop Compensators				Four compensators/filters are provided to optimize the circuit's THD response. Configure the low-power threshold in the ***Power Settings***.

1a	Current-Loop Low Line	0xFE29 0xFE2A	[7:0] [7:0]	R/W R/W	Sets the current-loop filter gain for low-line input. Sets the current-loop filter zero for low-line input.
1b	Current-Loop Low Line Light Load	0xFE90 0xFE91	[7:0] [7:0]	R/W R/W	Sets the current-loop filter gain for low-line input and light load. Sets the current-loop filter zero for low-line input and light load.
1c	Current-Loop High Line	0xFE2B 0xFE2C	[7:0] [7:0]	R/W R/W	Sets the current-loop filter gain for high-line input. Sets the current-loop filter zero for high-line input.
1d	Current-Loop High Line Light Load	0xFE92 0xFE93	[7:0] [7:0]	R/W R/W	Sets the current-loop filter gain for low-line input and light load. Sets the current-loop filter zero for low-line input and light load.
1e	Additional Settings: Current Loop V_{IN} Low Line V_{IN} High Line				Together with the circuit values defined in the GUI Main Screen, V_{IN} values are used to generate the corresponding Power Stage filter. If desired, set the low line and high line thresholds in the ***VAC Settings***.
1f/ 2c	Enable Feedforward	0xFE4F	[6]	R/W	The current-loop feedforward can be enabled to improve power factor and reduce THD, especially under light-load conditions.
	Voltage-Loop Compensators				Aside from the normal voltage compensator/filter, a fast voltage-loop compensator is provided for faster response during transient loading.
2a	Voltage Normal Loop	0xFE20 0xFE21	[7:0] [7:0]	R/W R/W	Sets the PFC voltage-loop filter gain. Sets the PFC voltage-loop filter zero.
2b	Voltage Fast Loop	0xFE22 0xFE23	[7:0] [7:0]	R/W R/W	Sets the PFC Fast voltage-loop filter gain. Sets the PFC Fast voltage-loop filter zero.
2c/ 1f	Additional Settings: Voltage Fast Loop Enable with Delay	0xFE24	[0] [4:2]	R/W R/W	Enables or disables the fast-loop filter with a delay.
2d					

2e	Fast-Filter to Normal-Filter Delay Normal-Filter to Fast-Filter Threshold		[6:5]	R/W	Sets fast-filter to normal-filter time delay after VOUT is inside the regulation band: 0 to 7 half AC cycles. Sets the threshold of the regulation band limit for switching from normal filter to fast filter: ±1.5625%, ±3.125%, ±6.25%, and ±12.5%.
	PLOT CONTROL				
3a 3b	Digital Filter Enable Digital Filter Plot and Adjustment				Enables or disables the gain and phase plots of the selected ***Digital Filter***. The green arrow on the ***Digital Filter*** plot can be moved to change the gain and zero of the compensator. Compensator values are applied to the ***Full Loop*** plot [6b] in real time to help with the control loops tuning.
4	Power Stage Filter Enable				Enables or disables the gain and phase plots of the ***Power Stage Filter*** relevant to the selected **Digital Filter**. The circuit values can be set on the ***Main GUI*** window.
5	Feedback Enable				Enables or disables the gain and phase plots of the ***Feedback Stage*** relevant to the selected ***Digital Filter***. The circuit values can be set on the ***Main GUI*** window.
6a 6b	Full Loop Enable Full Loop Plot				Enables or disables the gain and phase plots of the ***Full Loop*** of the selected ***Digital Filter*** to provide the crossover bandwidth that determines the circuit response. For a normal off-line application in the 50Hz/60Hz range, the voltage-loop crossover frequency is usually < 10Hz, while for the current loop, the crossover frequency is ~1kHz to 10kHz.
7	Apply Settings				Programs all the above values to the corresponding registers and bits.

Flag Settings

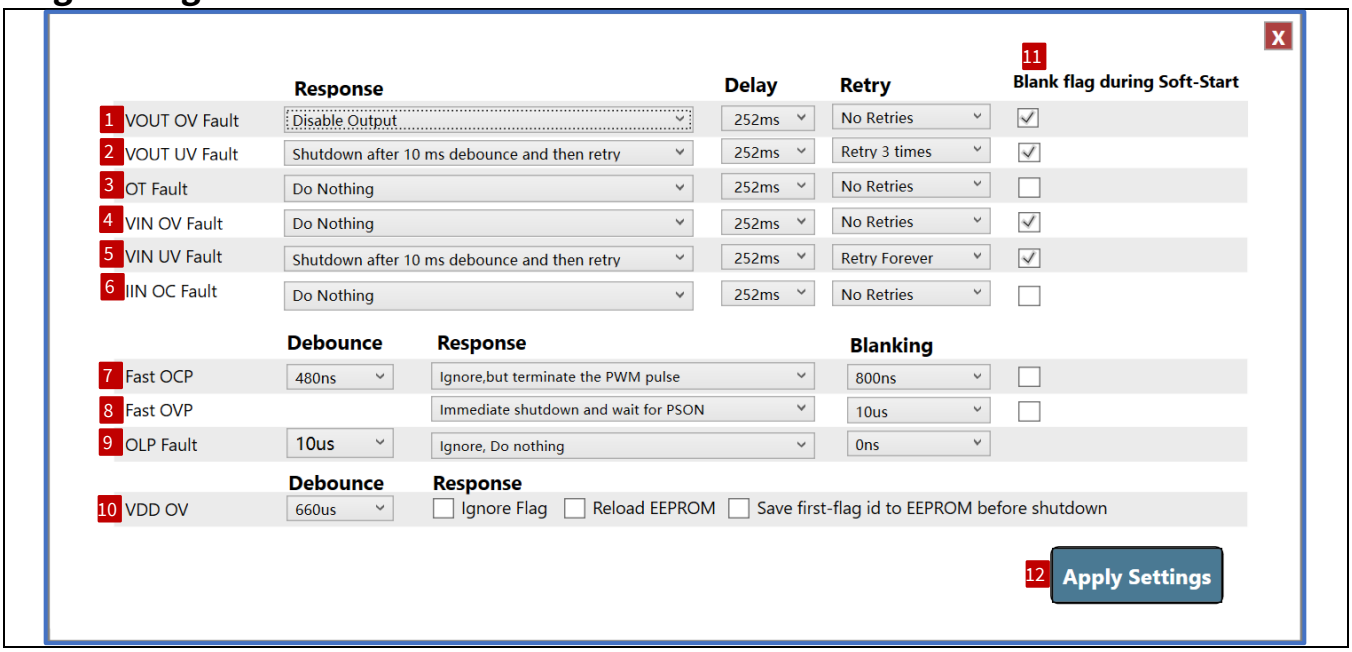

Figure 19. Flag Settings Navigation

Table 18. Figure 19 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	VOUT OV Fault	0x41			
	Response		[7:6]	R/W	Sets device response to an output overvoltage fault (OV) condition.
	Delay		[2:0]	R/W	Sets the delay before the output is disabled and the delay between restart attempts.
	Retry		[5:3]	R/W	Sets the number of retry attempts following a fault condition.
2	VOUT UV Fault	0x45			
	Response		[7:6]	R/W	Sets device response to an undervoltage fault (UV) condition.
	Delay		[2:0]	R/W	Sets the delay before the output is disabled and the delay between restart attempts.
	Retry		[5:3]	R/W	Sets the number of retry attempts following a fault condition.
3	OT Fault	0x50			
	Response		[7:6]	R/W	Sets device response to an overtemperature fault (OT) condition.
	Delay		[2:0]	R/W	Sets the delay before the output is disabled and the delay between restart attempts.
	Retry		[5:3]	R/W	

					Sets the number of retry attempts following a fault condition.
4	VIN OV Fault Response Delay Retry	0x56	 [7:6] [2:0] [5:3]	 R/W R/W R/W	Sets device response to an input overvoltage fault (OV) condition. Sets the delay before the output is disabled and the delay between restart attempts. Sets the number of retry attempts following a fault condition.
5	VIN UV Fault Response Delay Retry	0x5A	 [7:6] [2:0] [5:3]	 R/W R/W R/W	Sets the device response to an input undervoltage fault (UV) condition. Sets the delay before the output is disabled and the delay between restart attempts. Sets the number of retry attempts following a fault condition.
6	IIN OC Fault Response Delay Retry	0x5C	 [7:6] [2:0] [5:3]	 R/W R/W R/W	Sets the device response to an input overcurrent fault (OC) condition. Sets the delay before the output is disabled and the delay between restart attempts. Sets the number of retry attempts following a fault condition.
7	Fast OCP Debounce Response Blanking	 0xFE3D 0xFE00 0xFE3D	 [4:3] [7:6] [5:4] [2:0]	 R/W R/W R/W R/W	Sets the CS OCP debounce time. Sets the device response to a fast overcurrent-protection condition and the number of allowed switching cycles. Sets the leading-edge blanking time.
8	Fast OVP Debounce Response	0xFE31 0xFE01	 [1:0] [7:6]	 R/W R/W	Sets the fast overvoltage-protection (OVP) debounce time. Sets the device response to a fast-overvoltage condition. Blanking time is fixed at 10µs.
9	OLP Fault Response	0xFE02	 [7:6]	 R/W	Sets the device response to an open-loop (OLP) fault condition. Debounce time is fixed at 10µs, while blanking is 0ns.
10	VDD OV Debounce Response	0xFE03 0xFE04	 [1] [0]	 R/W R/W	Sets the VDD overvoltage (OV) debounce time: 2.56µs or 660µs.

			[2] [6]	R/W R/W	Sets to either the fault or not. Set whether to reload the EEPROM contents. Set to save first flag ID to EEPROM when device shuts down.
11	Blank Flag During Soft Start	0xFE08 0xFE09	[7:0] [0]	R/W R/W	Setting the checkbox means that corresponding flag is ignored until the end of the soft-start ramp time.
12	Apply Settings				Programs all the above values to the corresponding registers and bits.

Trim Settings

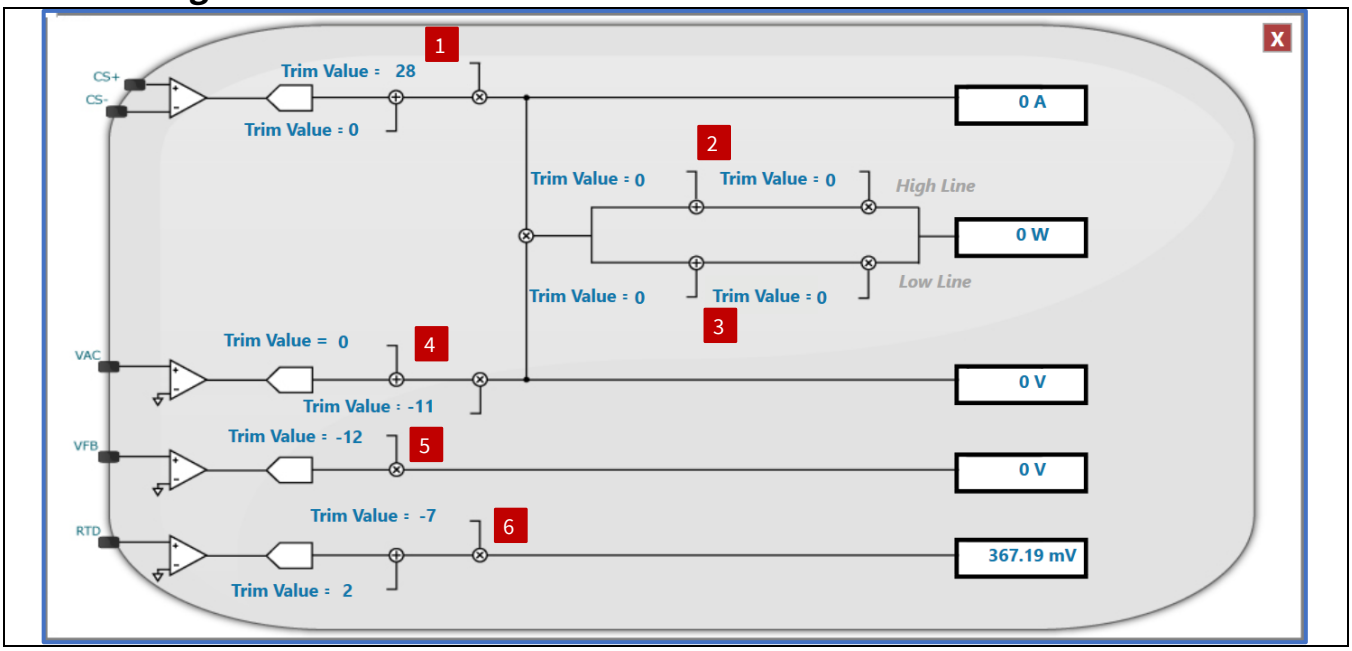

Figure 20. Trim Settings

Table 19. Figure 20 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Current-Sense Gain Trim Value				To update values, set write access on the ***GUI Control*** [9] to ***Unlock***.
		0xFE42	[7:0]	R/W	
	Offset Trim Value	0xFE7E	[7:0]	R/W	Calibrates the CS current-sense gain in the 500mV range.
		0xFE54	[7:0]	R/W	Calibrates the CS current-sense gain in the 750mV range.
		0xFE7F	[7:0]	R/W	Calibrates the CS current-sense offset in the 500mV range.
					Calibrates the CS current-sense offset in the 750mV range.
2	Power Metering HL Gain Trim Value	0xFE8F 0xFE8E	[7:0] [7:0]	R/W R/W	Calibrates the power metering gain for the high-line input voltage.

	Offset Trim Value				Calibrates the power metering offset for the high-line input voltage.
3	Power Metering LL Gain Trim Value Offset Trim Value	 0xFE34 0xFE33	 [7:0] [7:0]	 R/W R/W	 Calibrates the power metering gain for the low-line input voltage. Calibrates the power metering offset for the low-line input voltage.
4	VAC Sense Gain Trim Value Offset Trim Value	 0xFE40 0xFE53	 [7:0] [7:0]	 R/W R/W	 Calibrates the VAC voltage-sense gain. Calibrates the VAC voltage-sense offset.
5	VFB Sense Gain Trim Value	 0xFE41	 [7:0]	 R/W	 Calibrates the output voltage sense gain.
6	Thermistor Gain Trim Value Offset Trim Value	 0xFE18 0xFE16 0xFE17	 [7:0] [1:0] [7:0]	 R/W R/W R/W	Calibrates the RTD thermistor-sensing gain. This signed 9-bit value calibrates RTD thermistor-sensing offset.

Smart Voltage Settings

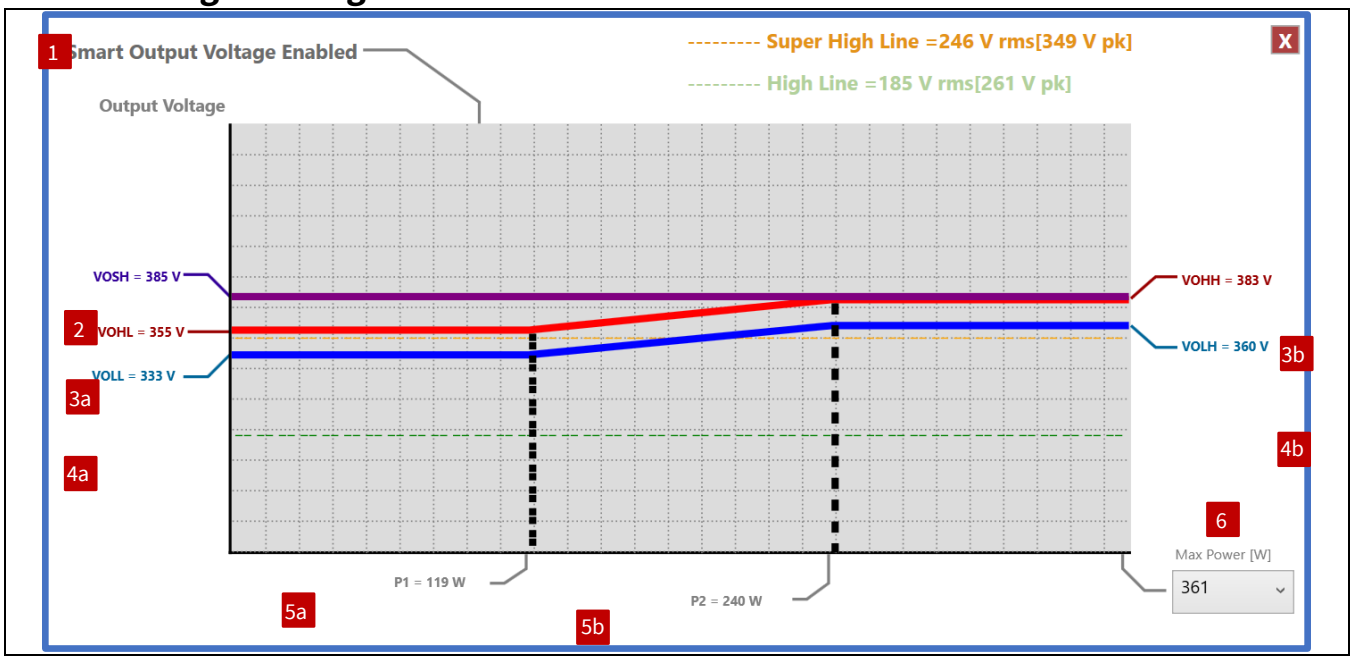

Figure 21. Smart Voltage Settings

Table 20. Figure 21 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION

1	Smart Output Voltage Enable	0xFE4F	[2]	R/W	Enables or disables the smart output voltage feature to achieve higher efficiency. This feature is not compatible for designs with a hold-up time requirement. Minimum value on the graph is set to 160V, which covers most applications. The maximum value is the same as the Max Range in ***VFB Settings***.
2	Super High Line VOSH	0xFE4A	[10:0]	R/W	Register value is ~3.325 * V_{SET}. It is usually same value as VOUT (0x21). Sets the output voltage when the input voltage VAC is higher than the value set in Register 0xFE4B or super high-line limit.
	High Line				Register value is ~3.325 * V_{SET}. Values must be higher than high-line limit.
3a	VOHL	0xFE48	[10:0]	R/W	Sets the output voltage under low-power operation with the high-line input.
3b	VOHH	0xFE49	[10:0]	R/W	Sets the output voltage under high-power operation with the high-line input.
	Low Line				Register value is ~3.325 * V_{SET}. Values must be higher than the low-line limit.
4a	VOLL	0xFE46	[10:0]	R/W	Sets the output voltage under low-power operation with the low-line input.
4b	VOLH	0xFE47	[10:0]	R/W	Sets the output voltage under high-power operation with the low-line input.
	Power Thresholds				Register values: ADP1047 is ~P_{SET}/1.41, the ADP1048 is ~P_{SET}/2.82.
5a		0xFE44	[12:0]	R/W	Values must be lower than the nominal PFC output power.
5b	VOP1 VOP2	0xFE45	[12:0]	R/W	Sets the lower-power operation threshold for the smart output voltage. Sets the high-power operation threshold for the smart output voltage.
6	Max Power				Sets the maximum range of power in Watts. ADP1047: 180W to 11,582W. ADP1048: 360W to 23,704W.

Temperature Settings

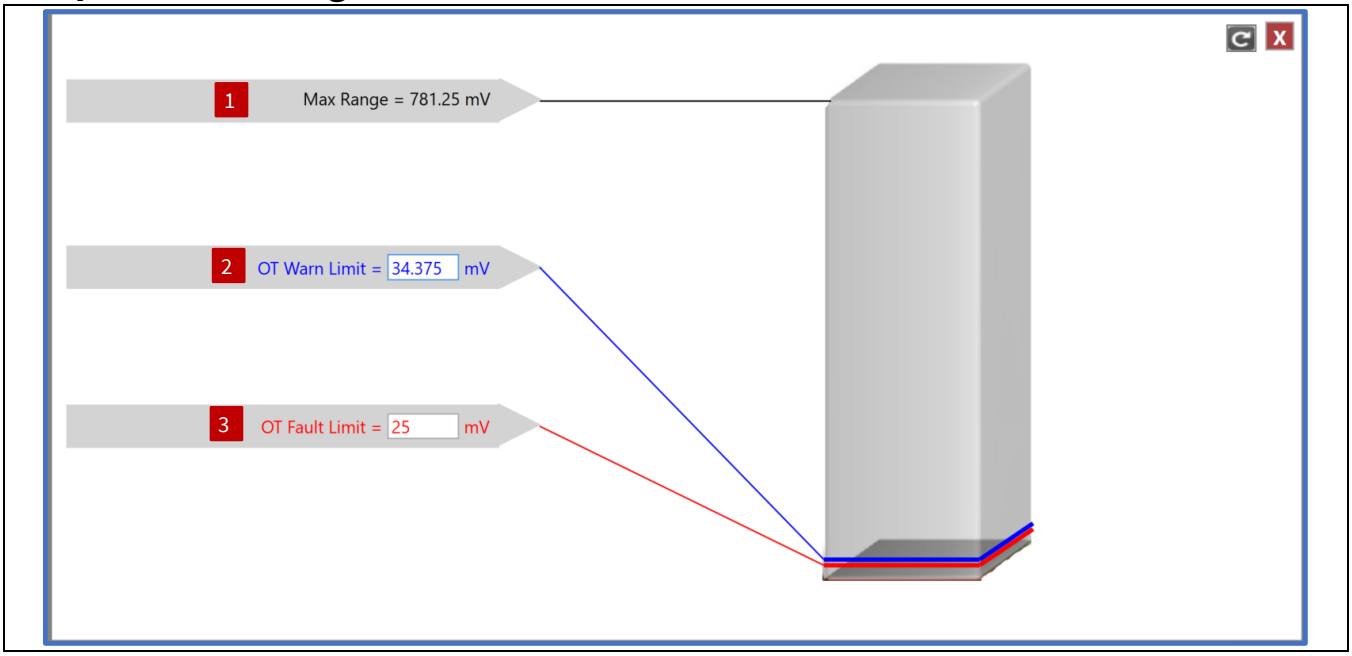

Figure 22. Temperature Settings Navigation

Table 21. Figure 22 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range				The RTD temperature ADC measurement is defined from the 0V to 0.8V RTD pin voltage. For readback, a 12-bit measurement is used through register 0xFE86. For temperature protection settings, only a 9-bit value is used in comparison. The allowed value for protection setting is between 9.375mV to 781.25mV in 3.125mV steps.
2	OT Warn Limit	0xFE1A	[7:0]	R/W	Overtemperature warning threshold. If the 9-bit RTD ADC is less than this register value, the overtemperature fault flag is set. Debounce time is 100ms. To set the value, either directly input the value or use the slider. Click ***Enter*** to confirm value change.
3	OT Fault Limit	0xFE19	[7:0]	R/W	Overtemperature fault threshold. If the 9-bit RTD ADC is less than this register value, the overtemperature warning flag is set. Debounce time is 100ms.

MONITOR

Main

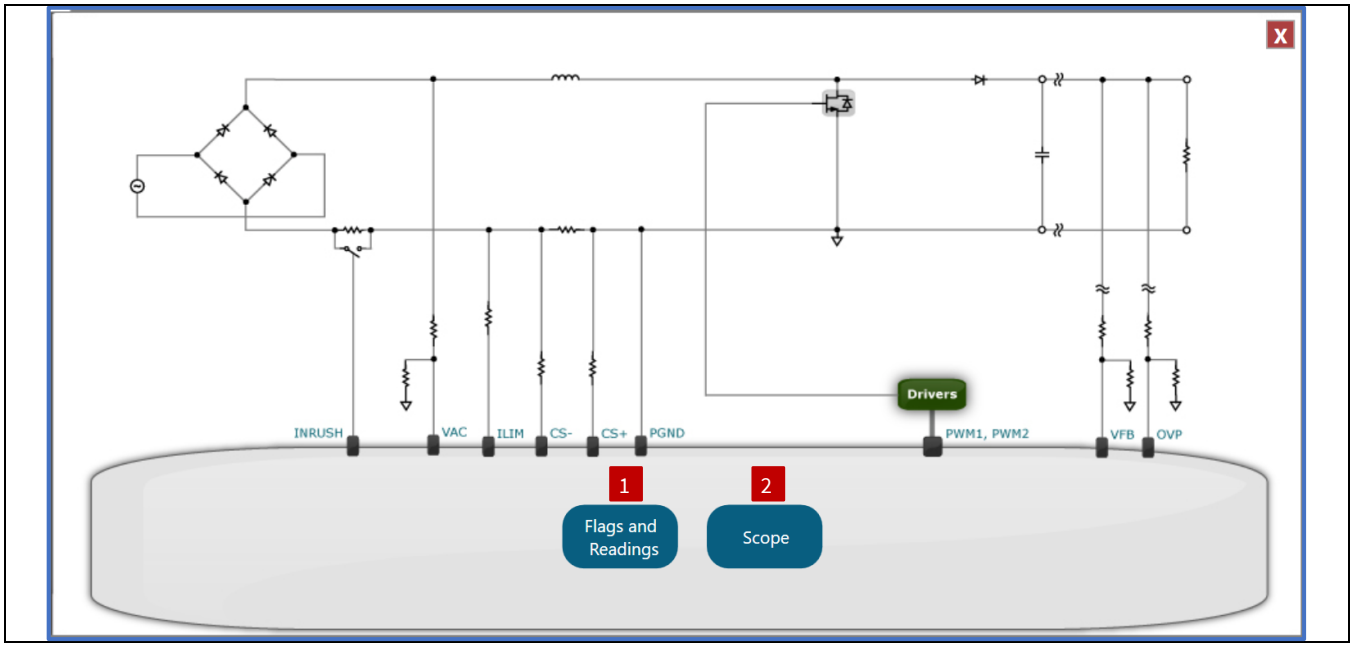

Figure 23. Main Navigation

Table 22. Figure 23 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Flag and Readings				The grey block represents the ADP1047 (or ADP1048), and the blue block represents its monitor blocks. Click this blue block to open its corresponding window for monitoring.
2	Scope				Opens the corresponding scope window.

Flags and Readings

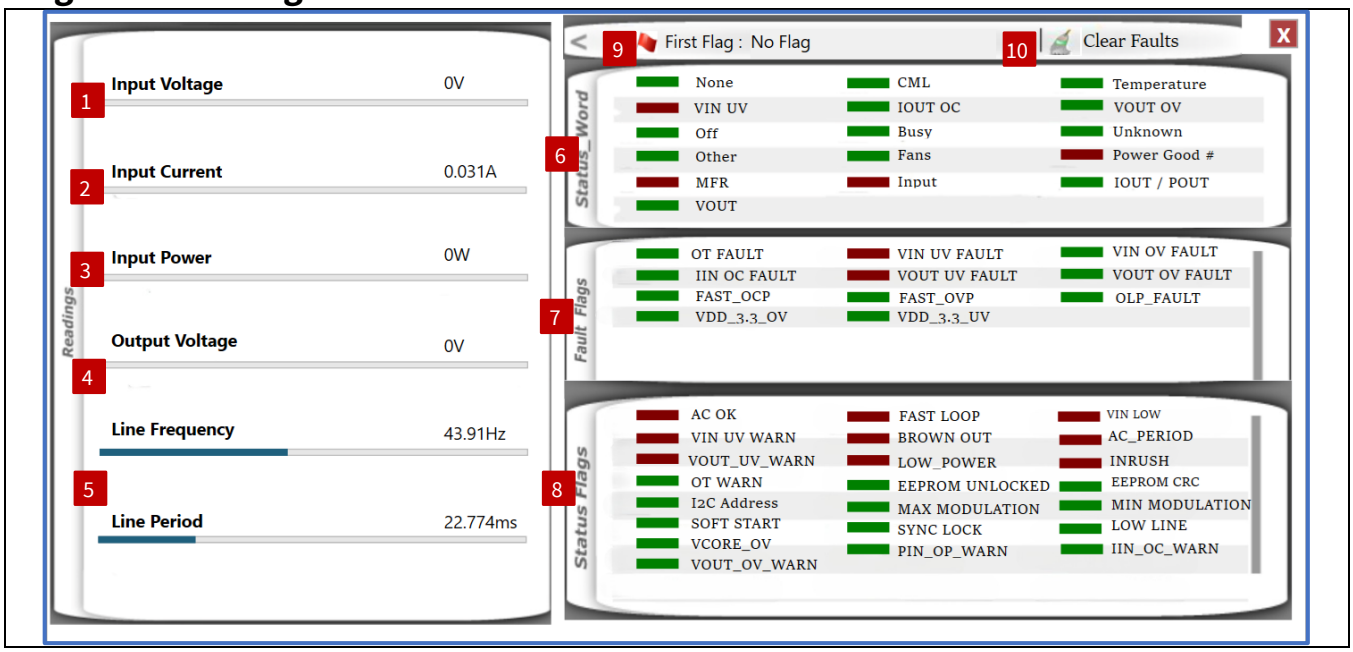

Figure 24. Flags and Readings Navigation

Table 23. Figure 24 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	READINGS Input Voltage Exponent N Mantissa	0x88	 [13:11] [10:0]	 R R	 Displays the measured input voltage in V_{RMS}. Displays the register value is in a linear mode format ($V = Y * 2^N$).
2	Input Current Exponent N Mantissa	0x89	[15:11] [10:0]	R R	Displays the measured input current in A_{RMS}. Displays the register value is in a linear mode format ($I = Y * 2^N$).
3	Input Power Exponent N Mantissa	0x97	[13:11] [10:0]	R R	Displays the input power in watts. Displays the register value is in a linear mode format ($P = Y * 2^N$).
4	Output Voltage Exponent N Mantissa	0x8B	[13:11] [10:0]	R R	Displays the output voltage in volts. Displays the register value is in a linear mode format ($V = Y * 2^N$).
5	Line Frequency Line Period	0xFE85 0xFE27	[7:0] [7:0]	R R	Displays the frequency based on the measured period of the VAC pin signal. If the measured period is outside the set

		0xFE28	[7:0]	R	range, the value is clamped to either the minimum AC period or the maximum AC period. Each register LSB corresponds to 163.84µs.
6	STATUS WORD	0x79			
	None		[0]	R	Red = Fault or warning is not listed in Bits[7:1].
	CML		[1]	R	Red = Communications, memory, or logic fault.
	Temperature		[2]	R	Red = Temperature fault or warning.
	VIN UV		[3]	R	Red = Output undervoltage fault.
	IOUT OC		[4]	R	Red = Output overcurrent fault.
	VOUT OV		[5]	R	Red = Output overvoltage fault.
	Off		[6]	R	Red = Device is not providing power to the output.
	Busy		[7]	R	Red = Device is busy and unable to respond.
	Unknown		[8]	R	Red = Fault or warning is not listed in Bits[15:1].
	Other		[9]	R	Always reads as 0 (green).
	Fans		[10]	R	Red = Fan or airflow fault or warning.
	Power Good#		[11]	R	Red = POWER_GOOD is negated.
	MFR		[12]	R	Red = Manufacturer-specific fault or warning.
	Input		[13]	R	Red = Input voltage, input current, or input power fault or warning.
	IOUT/POUT		[14]	R	Red = Output current or output power fault or warning.
	VOUT		[15]	R	Red = Output voltage fault or warning.
7	FAULT FLAGS				
	OT FAULT	0x7D	[7]	R	Red = Overtemperature fault.
	VIN UV FAULT	0x7C	[4]	R	Red = Input undervoltage fault.

	VIN OV FAULT	0x7C	[7]	R	Red = Input overvoltage fault.
	IIN OC FAULT	0x7C	[2]	R	Red = Input overcurrent fault.
	VOUT UV FAULT	0x7A	[4]	R	Red = Output undervoltage fault.
	VOUT OV FAULT	0x7A	[7]	R	Red = Output overvoltage fault.
	FAST OCP	0xFE81	[2]	R	Red = The comparator threshold on the ILIM pin has been crossed.
	FAST OVP	0xFE80	[4]	R	Red = The comparator threshold on the OVP pin has been crossed.
	OLP FAULT	0xFE80	[5]	R	
	VDD 3.3 OV	0xFE82	[2]	R	Red = One of the voltage dividers likely has opened.
	VDD 3.3 UV	0xFE82	[1]	R	Red = An overvoltage condition is present on the VDD rail.
					Red = An undervoltage condition is present on the VDD rail.
8	STATUS FLAGS				
	AC OK	0xFE81	[0]	R	Red = The output of the AC_OK pin is low.
	FAST LOOP	0xFE82	[4]	R	Red = The fast-loop compensation filter is in use.
	VIN LOW	0x7C	[3]	R	Red = The device is off due to insufficient input voltage.
	VIN UV WARN	0x7C	[5]	R	Red = Input undervoltage warning.
	BROWN OUT	0xFE80	[2]	R	Red = The input is lower than VIN_ON.
	AC PERIOD	0xFE80	[3]	R	Red = If an AC line period cannot be detected, the Max Period is used.
	VOUT UV WARN	0x7A	[5]	R	Red = Output undervoltage warning.
	LOW POWER	0xFE82	[5]	R	Red = The input power is below the low-power operation threshold.
	INRUSH	0xFE80	[0]	R	Red = The inrush relay is off.
	OT WARN	0x7D	[6]	R	Red = Overtemperature warning.

	EEPROM UNLOCKED	0xFE81	[6]	R	Red = The EEPROM is unlocked, and its contents can be written.
	EEPROM CRC	0xFE81	[5]	R	Red = The downloaded contents of the EEPROM are incorrect.
	I2C ADDRESS	0xFE81	[4]	R	Red = The address falls too close to the threshold between two addresses.
	MAX MODULATION	0xFE80	[7]	R	Red = The maximum modulation limit is reached.
	MIN MODULATION	0xFE80	[6]	R	Red = The minimum modulation limit is reached.
	SOFT START	0xFE80	[1]	R	Red = The system is in soft-start sequence.
	SYNC LOCK	0xFE81	[1]	R	Red = The external frequency synchronization is locked.
	LOW LINE	0xFE81	[3]	R	Red = The input voltage is higher than the high-line threshold.
	VCORE OV	0xFE82	[3]	R	Red = The overvoltage condition is present on the VCORE rail.
	PIN OP WARN	0x7C	[0]	R	Red = Input overpower warning.
	IIN OC WARN	0x7C	[1]	R	Red = Input overcurrent warning.
	VOUT OV WARN	0x7A	[6]	R	Red = Output overvoltage warning.
9	First Flag	0xFE07	[3:0]	R	Returns the fault ID of the fault that triggers the system to shut down.
10	Clear Faults	0x03			Sends a Clear Faults command.

Scope

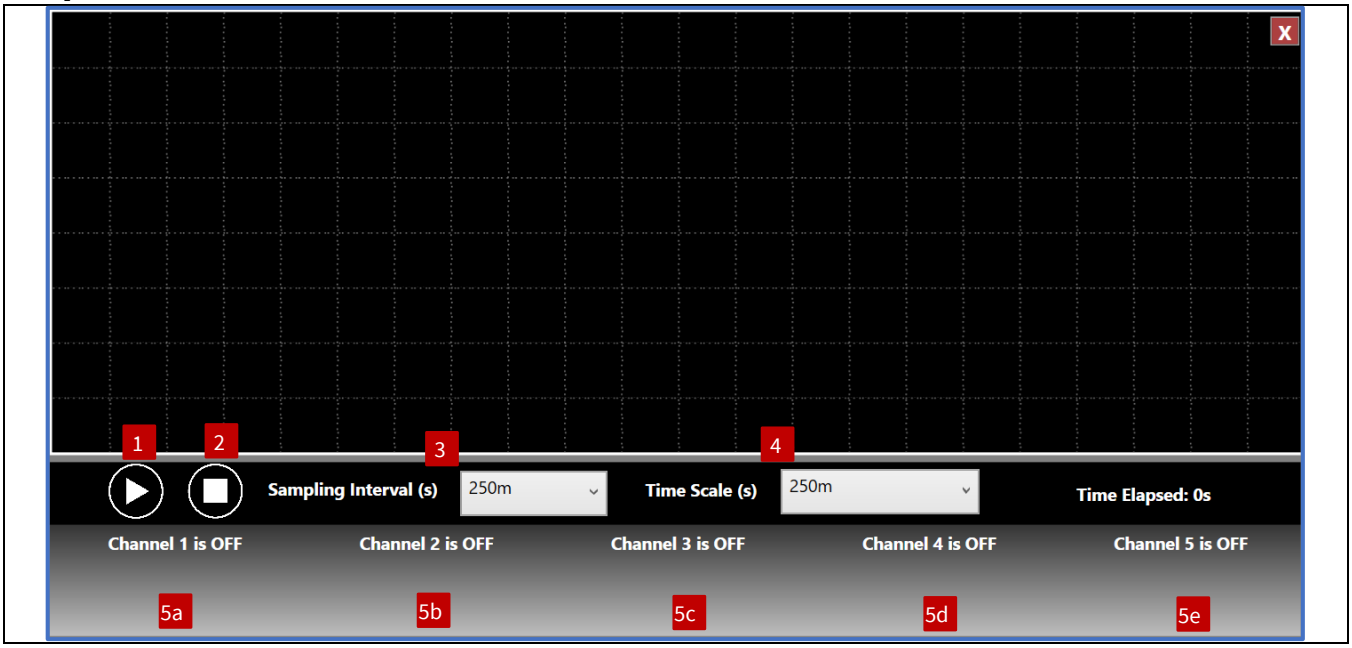

Figure 25. Scope Navigation

Table 24. Figure 25 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Start/Pause				Starts graphing the parameters configured on the channel over time. Press the button again to pause graphing.
2	Stop				Stops graphing and clear the display.
3	Sampling Interval				Sets the sampling interval.
4	Time Scale				Sets the time scale.
5 a–e	Scope Channels: Channel 1 to 5				Configures the parameters for each channel. Can be either one of the 5 readings or one of the 45 flags. Once the channel is configured, the parameter value, scale, and offset is displayed on the channel area.

REGISTER ACCESS

Main

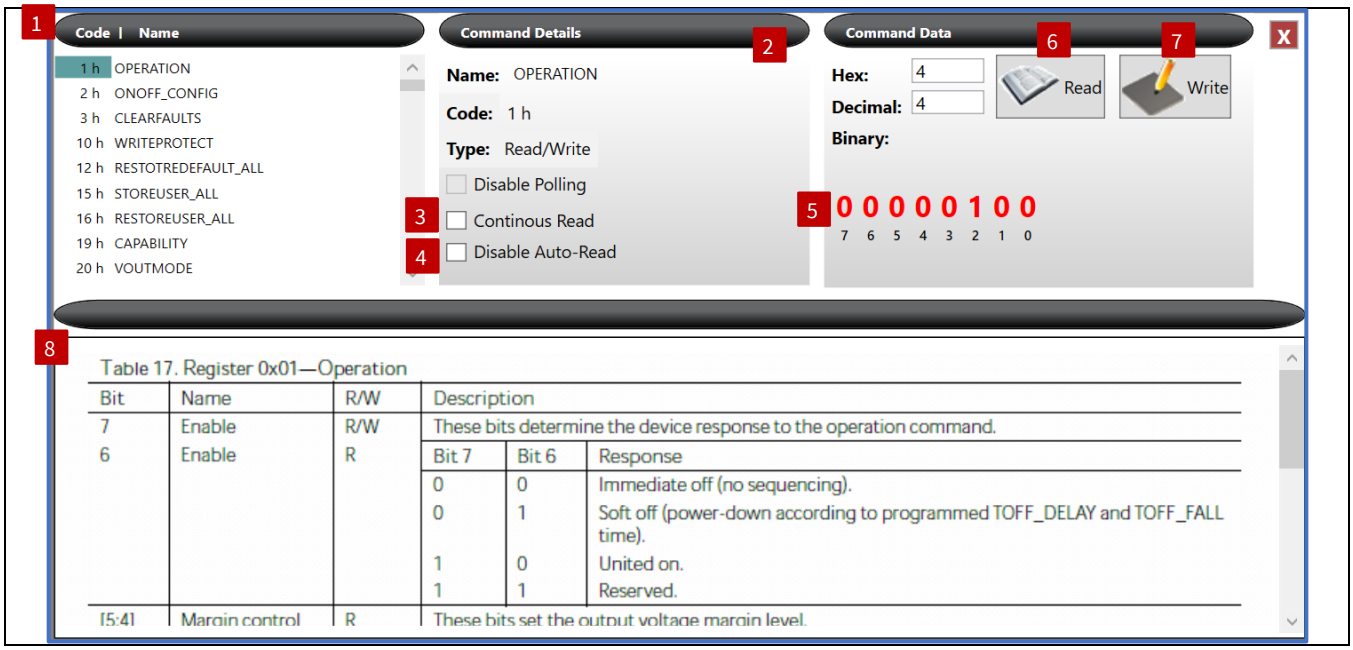

Figure 26. Main Navigation

Table 25. Figure 26 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Register Map	0x01–0xFE9B			Displays the complete ADP1047/ADP1048 register map. Selecting any register displays the data contained in that register and allows this register to be read and written to.
2	Register Details				Displays the selected register's Command Name, Code, and its value in hexadecimal and decimal formats.
3	Continuous Read				If this checkbox is enabled, the GUI continuously reads the value of the register selected.
4	Disable Automatic Readback				Automatically performs a read operation after a write operation to verify if the write operation was successful. Enabling this checkbox disables this automatic readback feature.
5	Bit Display				Displays the current value of the selected register, which can be modified by clicking on the individual bits.
6	Read				Reads the value of the selected register.
7	Write				Writes the value to the selected register.
8	Description				Displays the description of the selected register.

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
A	01/07	—	—
B	01/25	Updated General Description, title, added UG designation Updated Figures 1–26 Updated Tables 1–25	1–43