CrossCore® Development Tools by Analog Devices

Release Notes for CrossCore® Embedded Studio Rel.3.1.0-ga

1 Table of Contents

2 Introduction

This document describes the changes for CrossCore Embedded Studio (CCES) 3.1.0-ga. You can find the release notes for older releases in the `docs` sub-directory of your CCES installation as well as an Installation Guide which will help you install this release.

> The "-ga" in version "3.1.0-ga" is a quality level and indicates General Availability to denote a stable, reliable release suitable for widespread use.

For information on Linux please refer to the general Linux documentation Linux for ADSP-SC5xx Processors [Analog Devices Wiki]. Other useful links for CrossCore and Linux Development are:

- http://www.analog.com/cces-quickstart
- EngineerZone > Processors and DSP > Software and Development Tools > CrossCore Embedded Studio and Add-ins
- EngineerZone > Processors and DSP > Software and Development Tools > CrossCore Embedded Studio and Add-ins > tags > CCES
- EngineerZone > Processors and DSP > Software and Development Tools > CrossCore Embedded Studio and Add-ins > tags > CCES 3.1.0
- How to debug SHARC cores in CCES while running Linux
- Configuring System Memory for the ADSP-SC5xx When Using Linux and SHARC Applications

For information regarding support for ADuCM302x, ADuCM4x50 and ADuCM36x families of Arm Cortex-M microcontrollers the links below may be useful:

- https://wiki.analog.com/resources/eval/user-guides/eval-adicup3029
- https://wiki.analog.com/resources/eval/user-guides/ev-cog-ad3029lz
- https://wiki.analog.com/resources/eval/user-guides/ev-cog-ad4050w
- https://wiki.analog.com/resources/eval/user-guides/eval-adicup360

3 New and Noteworthy in CCES 3.1.0-ga

3.1 New SHARC-FX Processor Support

CrossCore Embedded Studio 3.1.0 introduces comprehensive support for the new ADSP-SC846 SHARC-FX processor family parts. This digital signal processor architecture expands the available target options for embedded development projects.

- ADSP-21844 / ADSP-21844W
- ADSP-21846 / ADSP-21846W
- ADSP-SC844 / ADSP-SC844W
- ADSP-SC846 / ADSP-SC846W

The new parts support is for **silicon revision 0.1** and verified using **`EV-SOMCRR2-EZKIT`** and **`EV-SC846-SOM`** evaluation boards and also **QEMU** and **Xtrun** simulation support.

The **EV-SC84x EZ-KIT Board Support Package (BSP)** is also available to download and install examples for the new parts.

3.2 Migrating an Existing SHARC+ Project to SHARC-FX

Support to migrate SHARC+ projects using CCES is available for the new ADSP-SC846 family parts similar to the support provided initially in CCES 3.0.0 for ADSP-SC835 family parts. See "Migrating an Existing SHARC+ Project to SHARC-FX" topic in the CCES help for further details.

Note: if adi_initialize.h is missing, right-click the system folder of the migrated project, select "Generate Add-in Initialization Source Files", clean and build the project again.

3.3 System Services and Device Drivers Support for ADSP-SC84x/ ADSP-2184x

The following Device Drivers and System Services are supported in this CCES release for the ADSP-SC846 family of parts. On the SHARC-FX & A55 cores, these can be added to the project using the Add-in via system.svc, or they can be referenced from the pre-built libdrv/libssl libraries provided.

Drivers	Services

• ASRC • CAN-FD (automotive parts only) • CRC • Crypto (PKA, PKTE ,TRNG) • EMAC • EMSI • FIR • HSM • HADC • IIR • Link Port • MLB (automotive parts only) • Rotary Counter • SPDIF Rx • SPDIF Tx • SPI • SPORT • TMU • TWI • UART • xSPI	• ARM-TMR • DAI • DMA (MDMA, EMDMA) • FPLL • GPIO • Interrupts • L2CTL • MEPU • PCG • PDM • PDMA • PKIC • PMU (GIC,ARM) • PWM • PWR • RCU • SMPU • SPU • SWU • TMR • TRU • WDT

Highlights for SSLDD:

- The FPLL service has been updated to include functionality for managing both FPLL0 and FPLL1 instances on ADSP-SC84x/2184x processors.
- The xSPI Open API (adi_xspi_Open) now includes support for handling multiple xSPI device instances through a device number parameter on ADSP-SC84x/2184x processors.
- Hardware Security Module-HSM driver support has been added for ADSP-SC84x/2184x processors.

Known issues/disclaimers for SSLDD

- The xSPI driver now requires the configuration macro ADI_XSPI_LOOP_OPTIMIZE_EN. Projects created with CCES 3.0.x may fail to build in CCES 3.1.0 unless this macro is explicitly defined.
- The xSPI driver for ADSP-SC835/SC846/21568 family of processors supports NOR Flash, HyperFlash, HyperRAM, and OctalRAM . NAND Flash memory is currently not supported.

3.4 OpenOCD Debugging Support for ADSP-SC84x/ADSP-2184x

ICE-1000/ICE-1500 Voltage with ADSP-SC84x/ADSP-2184x

Update the voltage to 1.8v by changing a jumper when using the ICE-1000 or ICE-1500 debug probes. Consult the ICE-1000 user guide or ICE-1500 user guide for more detailed information on changing the jumper.

The following limitations and requirements apply when using OpenOCD for debugging the new SHARC-FX processors (ADSP-SC84x/ADSP-2184x):

- **Preloads Required when loading to DDR**: You must run preloads first if any of the cores will be loading application code into DDR (this is the default for ARM cores); do not reset prior to loading any of the cores. The best option is to use the launch group wizard by selecting ***Application with CrossCore Launch Group*** and then clicking new (). The preloads will automatically be selected when proceeding in this way.
- *Creating an* ***Application with CrossCore Launch Group*** session now allows binary/exe/ project selection in the final step of the wizard. When selecting what to run on each core, you have a finer grained control over what is added when created.
- ADSP-SC84x/ADSP-2184x silicon is incompatible with the **ICE-2000.**

3.5 Multi Processor Debugging Support

CCES 3.1.0 adds supports for multi processor debug sessions. To create a multi processor debug configuration, you are provided the option at the beginning of the Launch Group Wizard. This feature was introduced mainly to support the `EV-SOMCRR2-EZKIT` when using two `EV-SC846-SOM` evaluation boards connected.

Features of this are as follows;

- Creating and name a launch group parent.
- Add existing debug group launches for a processor to the chain.
- Create and edit new group for each target processor using the existing Wizard tools.
- Add Bypass groups for skipping processors in the multi processor debug chain.

3.5.1 EV-SOMCRR2-EZKIT Single Processor vs Multi-Processor Debug Connection with Debug Agent

The EV-SOMCRR2-EZKIT can be configured for 1 or 2 ADSP-SC846 SOMs. When configured for 1, users should choose the **Analog Devices Onboard Debug Agent** interface when creating the debug configuration. When configured for 2, users should choose the **Analog Devices Onboard Multi-Processor Debug Agent** interface.

3.6 Flashing ADSP-SC83x/ADSP-2183x External Memory with adsp21835w_ev_ezkit.cfg vs adsp21835w_ev_som.cfg

To flash the external memory that is located on the `ADSP83x/ADSP2183x-EV-SOM` board, the `adsp21835w_ev_som.cfg` board file should be used. Current support includes:

- `issi25lp512m` via SPI
- `s26kl512s` via xSPI

To flash external memory located on the `EV-SOMCRR-EZKIT` board the `adsp21835w_ev_ezkit.cfg` should be used. Current support includes:

- `mx66u1g45g` via xSPI

3.7 Updated Xtensa Toolchain for SHARC-FX Processor Family

The Xtensa toolchain has been updated in CCES 3.1.0 to provide support for the complete SHARC-FX processor family,
including both existing ADSP-SC83x/ADSP-2183x parts and the new ADSP-SC84x/ADSP-2184x processors.

Xtensa Software Tools v15.05 Enhancements:

- Xtensa Software Tools version 15.05 includes a preview version of Extra Clang Tools (most notably clang-tidy and clangd) in the `XtensaTools/llvm/bin` directory. For documentation, please refer to https://clang.llvm.org/extra/index.html.
- The xt-clang compiler now issues a warning when the same variable is passed to multiple out or inout arguments of a TIE intrinsic function (aka TIE proto).
- The `xtutil` library now provides a random number generation function. This enables an application to generate the same sequence of pseudorandom numbers regardless of the choice of C library.
- A new function `idma_release_loop_buffer()` has been added to the IDMA library, to enable freeing up of channel buffer slots for multi-threaded applications.
- Added new user-visible HAL APIs `xthal_interrupt_sens_set_level()` and `xthal_interrupt_sens_set_edge()`. Added new convenience defines `XTHAL_INTERRUPT_SENS_EDGE` and `XTHAL_INTERRUPT_SENS_LEVEL` for use with existing `xthal_interrupt_sens_set()` API.
- The Xtensa Processor Hardware Abstraction Layer (HAL) includes instruction cache invalidate functions that only invalidate the portion of the cache that has appropriate execute permissions (X on MPU).
- The XTOS Power Shut Off (PSO) support functions are being replaced by equivalent HAL functions. While the XTOS functions are still available, they are now deprecated and will be removed in a future release. They now call the HAL functions internally. For more information, refer to the Xtensa®System Software Reference Manual.
- This release includes a pthreads-compatible interface library for XOS, allowing pthread based applications to be ported to XOS. For more information see the Xtensa® XOS Reference Manual.

Xtensa Software Tools v15.05 Fixes:

- A bug in a previous release of linker script generation caused the size of the "l2ram" memory region in the memory map to be half of the configured L2 size. This has been fixed.
- A previous release of the xt-clang compiler could crash when used with precompiled header files. This issue has been fixed.
- A previous release of xt-objdump could generate spurious warnings "DWARF error: could not find variable specification at offset" when disassembling Xtensa object files. This issue has been fixed.
- The xt-genmpu tool was generating incorrect MPU table entries if the memory region start or end address was not aligned to the MPU minimum region size. Such entries get truncated when programmed into the hardware and can lead to incorrect behavior and crashes. This has been changed.
- Now the MPU table is not generated if such regions are encountered in the memory map, a warning message is displayed. An LSP with such a memory map will still have correct linker scripts, but will not have the generated mpu_table.c file and corresponding library. The MPU

will be programmed with the fallback option of using the symbol `_memmap_cacheattr_reset` to create 8 regions of 512 MB each.
- A bug in a previous release of xt-gdb could cause it to crash when trying to print custom TIE types cast to standard integer types. This has been fixed.
- Both xt-gdb and Xtensa Xplorer displayed IDMA registers only for the first channel, if more than one channel was configured. This has been fixed.

3.8 Enhanced Boot and Security Tools

3.8.1 Updated Elfloader Utility

The elfloader utility has been enhanced with new capabilities for SHARC-FX processors:

- **DDR Miniloader Support**: Enables customized DDR memory setup during boot. This does however need to be configured manually and provided in binary format.
- **Hardware Security Module (HSM) Integration**: Support for HSM configuration and execution
- **Boot Optimisation**: Improved BootROM buffer management and memory protection for faster boot times
- **Enhanced Signing Support**: Better alignment and separation options for secure boot workflows

3.8.2 Updated adi_signtool

The signing tool now supports version 4 secure headers with new features:

- **xSPI Boot Support**: Enhanced support for xSPI boot modes with configurable PHY and training Data
- **SC84x Family Support**: Expanded secure header attributes and configuration options
- **HSM Integration**: Streamlined workflow for combining HSM and main encrypted program images

For detailed usage instructions, refer to the CCES 3.1.0 User Guide and tool documentation.

3.9 Updated Cortex-M33 Toolchain for ADSP-SC83x and ADuCM CMSIS packs support

The GCC arm embedded toolchain as used for the ADSP-SC83x processors and the various ADuCM CMSIS packs has been updated.

- GNU ARM Embedded Toolchain: Updated to version 13.2.1
  - For detailed changes, refer to: GCC 13 Changes
- GNU ARM Embedded Binutils: Updated to version 2.41
  - For detailed release notes, refer to: Binutils 2.41 Release Notes

Note: Existing projects may require updates to address new warnings or enhanced error checking introduced by the updated toolchain components.

3.10 Updated Cortex-A toolchains for ADSP-SC5xx

The GNU ARM Toolchains used for Cortex-A5 and Cortex-A55 ADSP-SC5xx parts ARM cores have been updated to version **14.3,** which includes the following components:

- Updated GCC to source code based on version **14.3**.
- Updated Binutils to source code based on version **2.44**.
- Updated GDB to source code based on version **15**.
- Updated Glibc to source code based on version **2.40**
- Updated Newlib to source code based on trunk.
- Updated Libexpat to source code based on version **2.7.1**

Note: Existing projects may require updates to address new warnings or enhanced error checking introduced by the updated toolchain components.

3.11 Noteworthy bugs fixed in CCES 3.1.0

- Can't view ADSP-SC594 flash memory used by SPI2 for XIP
- "Internal Error" During Debug Launch of Core2 Debug Group on ADSP-SC598 at 2MHz
- ADSP-21568 stack and heap in xSPI configured as SRAM causes code also in xSPI to be corrupted before main
- SHARC+ parts interrupt dispatcher saves incompatible for FreeRTOS uses
- Errors attempting to add FreeRTOSfor SHARC add-in.

4 Known Issues in CCES 3.1.0

4.1 Compatibility Note – Terminology Updates

Several drivers, services, and device header files for the ADSP-SC835 and ADSP-SC846 processor families have been updated to use modern, culturally appropriate terminology. As a result, existing projects may require source code changes when migrating to CCES 3.1.0. For details, refer to the affected header files under `Xtensa/SHARC-FX/include/drivers` and `Xtensa/SHARC-FX/include/services`.

4.2 False Semantic Errors

A small proportion of projects for the new ADSP-SC846 family parts show semantic errors for adi_core.h core macros in the generated main() source but still build successfully. An example of this error would be `"Symbol 'ADI_CORE_SHARC0' could not be resolved"` in the problems view but the projects builds successfully so clearly is defined. These false errors can be safely ignored.

4.3 GCC ARM Embedded Linker warnings for ADuCM36x, ADuCM302x, ADuCM4x50

The updated ARM embedded toolchain may generate linker warnings indicating that the `_read`, `_write`, `_lseek`, and `_close` functions are not implemented. These warnings are reported in the CCES as errors; however, the build completes successfully and the generated application is unaffected provided these functions are not used by the application.

No action is required unless your application relies on these functions, in which case user-provided implementations must be supplied

4.4 Creating Group Launch for SHARC/SHARC+ with projects for not all cores

When creating a Group Launch for a SHARC(+) part such as ADSP-SC598 where the Crosscore Debugger is to debug on Core2, with GDB and OpenOCD on Core0 and no workspace project is created for Core1. The group launch will be unable to create a Crosscore Debugger Configuration for you but can pickup and use a pre-configured session for Core2. This is due to the expected use case that a Core0 and Core1 project scenario would be used since it is the first core to be unlocked by the booting core.

4.5 Linker Warning: LOAD Segment with RWX Permissions (ARM Cores)

When building projects for ARM Cortex-M33, Cortex-A5 or Cortex-A55 cores, the GNU ARM Linker / GCC ARM Linker may issue the following warning:

```
<projectname>_Core<#> has a LOAD segment with RWX permissions.
```

- Cause: This warning results from security features introduced in GNU Binutils 2.39, which now appears in CCES due to the GNU ARM toolchains being updated.

- Workaround: This warning is disabled by default in new project but old projects may not be updated with the new project setting. You can disable this warning in the project Linker settings: `-Wl,--no-warn-rwx-segments`

4.6 Backward Compatibility for ADSP-SC83x/ADSP-2183x/ ADSP-21568 xSPI Projects

xSPI driver has been updated with certain Enums/Structures/Macros/API for ADSP-SC83x/ADSP-2183x/ ADSP-21568 family of processors. The xSPI driver static configuration "adi_xspi_config_SC8xx.h/ adi_xspi_config_2156x.h" files have been updated.

Any ADSP-SC83x/ADSP-21568 family projects with the xSPI driver added using earlier versions i.e CCES-3.x.y may get certain warnings/errors while importing these examples projects in CCES-3.1.0. In case of any warnings, please refer to updated adi_xspi_config_SC8xx.h & adi_xspi_config_2156x.h files and update the application accordingly.

Steps to update your "adi_xspi_config_SC8xx.h/adi_xspi_config_2156x.h" are:

- Take a backup of xSPI static configuration "adi_xspi_config_SC8xx.h" file at "$project/ system/drivers/xspi"
- Uninstall the xSPI addin from system.svc
- Re-install the xSPI add from system.svc
- Update the macros in the "adi_xspi_config_SC8xx.h/adi_xspi_config_2156x.h" file as per the backed-up file.

4.7 GDB Python 3.8 Dependency (gcc-arm-embedded toolchain)

The precompiled arm-none-eabi-gdb binary in the gcc-arm-embedded toolchain requires Python 3.8 to initialize properly. On systems where Python 3.8 is not installed, users may encounter a *ModuleNotFoundError: No module named 'encodings'* when launching GDB.

Workaround:

On Ubuntu 20.04; Python 3.8 is available in the official repositories. Install it with:

```
sudo apt install python3.8
```

On Ubuntu 22.04 and later; Python 3.8 is not available in the official repositories. Users can install Python 3.8 from the deadsnakes PPA as a workaround:

```
sudo add-apt-repository ppa:deadsnakes/ppa
sudo apt update
sudo apt install python3.8
```

After installing on any system, set **PYTHONHOME=/usr** in environment.

After updating the environment variable, restart your terminal or IDE session. GDB should then launch without errors.

4.8 Issue Combining Commands using Command Line Device Programmer

When programming flash on the ADSP-SC58x, ADSP-SC594 family, or ADSP-SC57x using core 0, the **info** command cannot be combined with other commands. This issue will also be seen when programming flash for the ADSP-SC83x and ADSP-SC84x processors.

4.9 Emulator and Debug Compatibility — ADSP-SC84x and ADSP-2184x

Please be advised that the ADSP-SC84x and ADSP-2184x processor families do not support all JTAG emulators. To establish a reliable debug connection, one of the supported configurations described below must be used.

Fully supported

- **On-board debug agent** — The `EV-SOMCRR2-EZKIT` integrated debugger is fully supported and provides the most straightforward and reliable means of connection.
- **ICE-1500 emulator** — Fully supported for external JTAG and debug operations, and is the recommended option where an external emulator is required.

Supported with limitations

- **ICE-1000 emulator** — Supported only when connected directly to the SOM board. Connection through any other point, such as a carrier or baseboard, is not reliable and is therefore not supported.

Not supported

- **ICE-2000 emulator** — Not compatible with the ADSP-SC84x and ADSP-2184x families and must not be used with these devices.

4.9.1 Compatibility Summary

Debug connection	Status	Notes
On-board debug agent	Fully supported	Recommended
ICE-1500	Fully supported	Recommended for external JTAG
ICE-1000	Supported with limitations	Reliable only when connected directly to the SOM board
ICE-2000	Not supported	Not compatible with ADSP-SC84x / ADSP-2184x

NOTE: Customers requiring assistance with a specific configuration, or with migration to a supported setup, should contact processor.tools.support@analog.com

4.10 ICE-2000 Maximum JTAG Frequency

The maximum JTAG frequency available to select for the ICE-2000 is 46 MHz but it may not work for all processors. Most ADI processors will work at a JTAG frequency up to ~30 MHz.

5 CCES License Keys for Evaluation

The purchase of many of the evaluation boards supported by CrossCore Embedded Studio (CCES) includes a complimentary EZK license key to enable use of CCES. These EZK license keys provide access to CrossCore Embedded Studio (CCES) and related development tools for your specific hardware platform to allow use of the evaluation board if you do not otherwise have a full CCES license. The various EZK license keys are copied below as a convenient reference.

5.1 SHARC/SHARC-FX Processors:

- EZK-CCES-ACHM-6VU9-Z4CP-FGV2-AXW5-UVKI-5N01 (ADSP-SC571 EZ-KIT)
- EZK-CCES-C92A-R9Q2-996X-HUHY-8IN5-4DXH-GS01 (ADSP-SC573 EZ-KIT)
- EZK-CCES-672Y-MB9T-D6RD-MQKC-M9CJ-7JN9-NA01 (ADSP-SC584 EZ-KIT)
- EZK-CCES-6NE5-HATV-93NS-BQA4-KFKZ-7QS4-GA01 (ADSP-SC584 EVAL-ADV7664-SMZ)
- EZK-CCES-ESCD-2F94-BAA5-BUJQ-YUW8-4I5S-CN01 (ADSP-SC589 EZ-KIT)
- EZK-CCES-9FYX-DSAC-FPNV-4WVP-E5X4-VGKC-GI01 (ADZS-SC589-MINI - SHARC A2X Main Board)
- EZK-CCES-8W56-QEI2-QZ8F-HHMC-325C-K7GF-ZA01 (ADSP-21569 EZ-KIT)
- EZK-CCES-J8AV-3UXX-KANT-2A8Q-WQFY-HUP9-Z601 (ADSP-SC594 SOM)
- EZK-CCES-J7TX-2HPZ-8ZDP-S4J5-UY27-TIQA-9S01 (ADSP-21593 SOM)
- EZK-CCES-9KC8-TSTX-V9IX-98NU-MNFF-V7I9-A201 (ADSP-SC598 SOM)
- EZK-CCES-HF24-2KZX-WGUM-VHGH-MJR6-IBFI-U201 (ADSP-21564 SOM)
- EZK-CCES-HU6H-ZAJ7-CV2K-GIAI-YPS4-B5AQ-I201 (ADSP-21568 SOM)
- EZK-CCES-GECM-GJDJ-MI6Q-UKEB-QCYM-NYV5-ZN01 (ADSP-21835W SOM)
- EZK-CCES-4Z7X-PHA2-Y4BM-2FJT-ECQB-RW4A-V601 (ADSP-SC835W SOM)
- EZK-CCES-CJB5-EF38-VQAV-FHRY-NXBQ-6B8U-IW01 (ADSP-21846W SOM)
- EZK-CCES-JIFW-68GQ-XEW7-A5QN-BCGB-IY6Y-UN01 (ADSP-SC846W SOM)

5.2 Cortex-M Processors:

- EZK-CCES-5JNP-FQH2-IAZZ-IJY4-E4HG-YIY6-JE01 (ADuCM360 CUP board - ADICUP360)
- EZK-CCES-RTC3-RPI5-WUEM-CJ9D-8DM4-GAR9-5E01 (ADuCM3029 EZ-KIT)
- EZK-CCES-QZJ9-PHY8-PWN5-2VEW-YMUB-HUI3-BW01 (ADuCM3029 CUP board - ADICUP3029)
- EZK-CCES-6XMG-BRRR-7CUS-K3AA-J92U-XK4A-2A01 (ADuCM3029 COG board - EV-COG-AD3029LZ)
- EZK-CCES-QCQ9-692E-TSCV-M9N6-A2NB-ZW8M-H201 (ADuCM4050LF EZ-KIT)
- EZK-CCES-YBS4-NX3P-EQR3-XEDE-9IN6-DJRJ-DW01 (ADuCM4050WL EZ-KIT)
- EZK-CCES-DWKV-QKPM-8Z9D-TRXE-8P4U-A57H-FE01 (ADuCM4050L COG board - EV-COG-AD4050LZ)
- EZK-CCES-VK6J-SI2H-89QM-77IU-7FWS-6UE4-7A01 (EVAL-ADPAQ3029EBZ - ADuCM3029)
- EZK-CCES-MSQH-GMIQ-ZB88-4XNV-53UH-52DE-4W01 (ADuCM3029 EZ-KIT)
- EZK-CCES-SIBY-5FXP-CPKG-7J8Z-DDHJ-KWZD-5601 (ADuCM3029 CUP board - ADICUP3029)
- EZK-CCES-PR39-4ZXD-4923-DUZ7-HKRW-69VI-JS01 (ADuCM4050LF EZ-KIT)
- EZK-CCES-Z4SS-3FRP-MXCD-ERET-Q92N-MWSK-EA01 (ADuCM4050WF EZ-KIT)

NOTE: Each serial number is tied to specific hardware and may have different licensing terms. Please use the appropriate serial number that corresponds to your purchased hardware. For questions about licensing or activation, please contact technical support - **processor.tools.support@analog.com**